As performance demands increase, logic device architecture is getting smaller and more complex. In the front end of line (FEOL), transistors are moving to non-planar 3D structures. In the back end of line (BEOL), metal line widths and pitch are shrinking. New choices in materials and processes are required to ensure device performance while improving yield and controlling costs. Each innovation yields new challenges and considerations downstream. It is likely a holistic approach is needed.

**FEOL: NEW ARCHITECTURES AND MATERIALS**

New architectures are being explored to improve transistor performance factors, which leads to new material considerations. Additionally, the intrinsic carrier mobility within the transistor must be improved using new channel materials such as silicon-germanium (SiGe) and germanium (Ge), which require new surface cleans, etch chemicals, and new high-k/channel interface layers.

**BEOL: NEW METALLURGIES AND PROCESSES**

As dimensions get smaller, the conductivity and reliability of traditional materials like tungsten (W) and copper (Cu) are no longer sufficient to enable performance and reliability.

**ENTEGRIS HOLISTIC SOLUTIONS FOR THE ENTIRE ECOSYSTEM**

Entegris holistically addresses every aspect of the fabrication process to improve device performance, yield, and reliability. From the source to the wafer, entegris offers solutions that enable the entire ecosystem.

**CLEANER MATERIALS ARE KEY**

As the number of process steps increase, cumulative yield drops significantly. As critical defect size decreases to below 10 nm, the total acceptable particle count also decreases.

**REO! NEW METALLURGIES AND PROCESSES**

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**ENTEGRIS HOLISTIC SOLUTIONS FOR THE ENTIRE ECOSYSTEM**

Only Entegris has the breadth of solutions and depth of industry expertise to enable our customers to transform radical ideas into modern technology.

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