Electrostatic Chuck Technology – Tailored Wafer Contact Surface Design and Application

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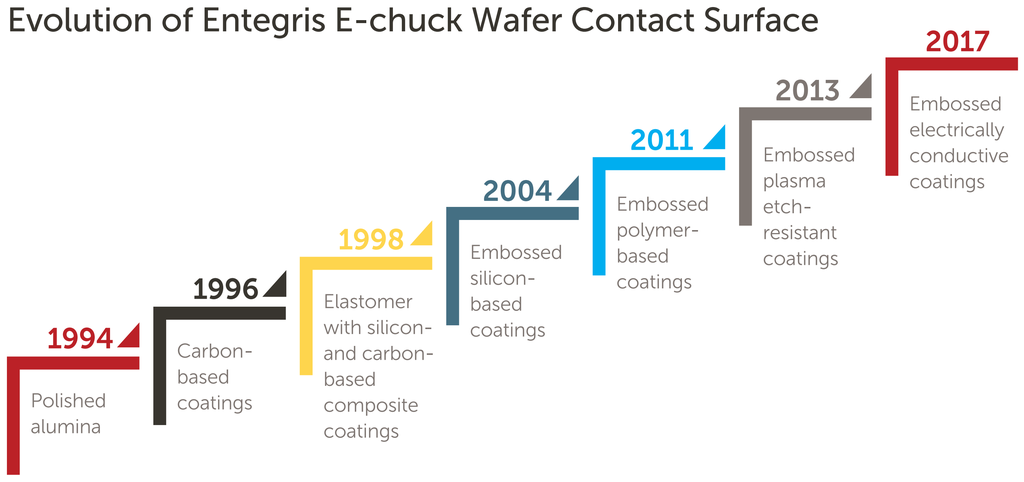
INTRODUCTION

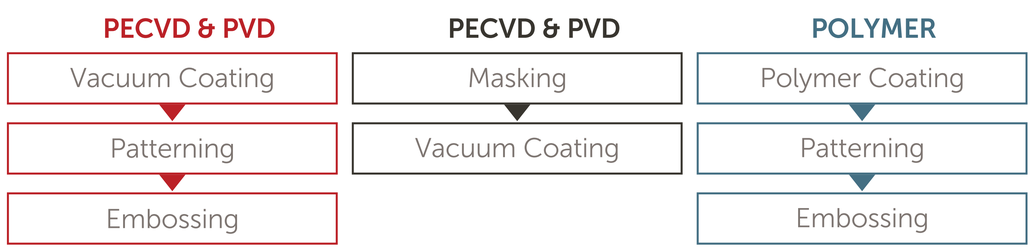
Wafer contact surface is the outer layer of material on electrostatic chuck (e-chuck) that directly contacts backside of wafer substrates in microfabrication process. It plays more and more important role as its material, structure and properties greatly affect e-chuck performance and device yield. Key characteristics for high performance e-chuck wafer contact surface include particle and metal generation, electrical conductivity for surface charge dissipation, thermal conductivity for backside gas cooling, oxidation and corrosion protection, wear resistance, adhesion enhancement and flatness stability etc. Traditionally, wafer contact surface is either dielectric front surface or patterned structure built out of dielectric layer. In contrast, Entegris developed new technologies to create unique separated wafer contact surface layer by various thin film deposition technologies — Plasma Enhanced Chemical Vapor Deposition (PECVD), Pegasus® (Physical Vapor Deposition, PVD) and polymer coatings, which provide advantage and flexibility to tailor material solution on e-chuck for requirements of advanced technology nods.

BACKGROUND

Evolution of Entegris E-chuck Wafer Contact Surface



METHODS

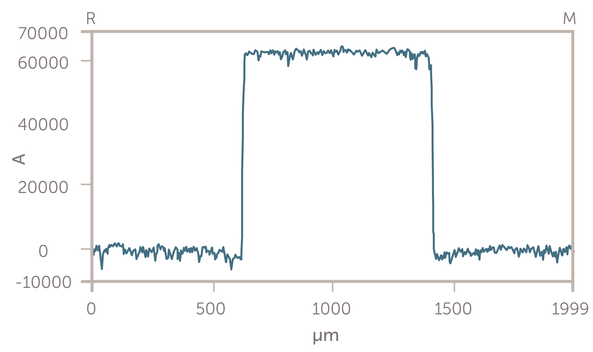


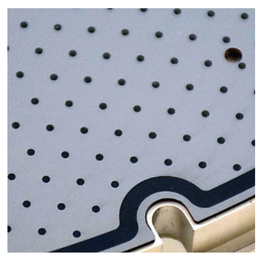
- Both PECVD and PVD wafer contact surfaces can be created by two processes:
  - — Coating followed by patterning and embossing
  - — Coating through physical mask system
  - — Technology and process are chosen based on wafer contact surface material selection best for e-chuck application
- Combination of above technologies possible for unique properties.
- Wafer contact surface coatings can be restored by refurbishment process.

RESULTS

Embossed Silicon-based Coating Wafer Contact Surface

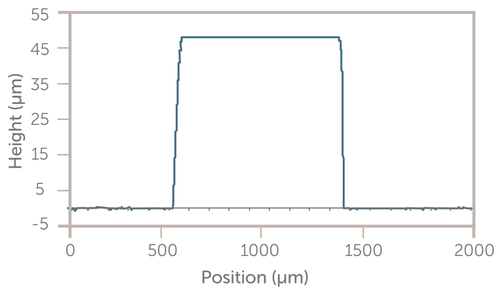
- Hard surface with embossment and seal ring structures that reduce total wafer contact area.
- Ultra-high purity amorphous surface with ultra-low particle and metal contamination.
- Specially design embossment pattern for minimizing wafer sagging under electrostatic clamping.
- Electrostatic dissipation (ESD) property to reduce risk of wafer sticking caused by residual surface charge.
- Hard surface can be cleaned by cleanroom wipe with cleanroom chemicals – DIW, IPA, acetone etc.





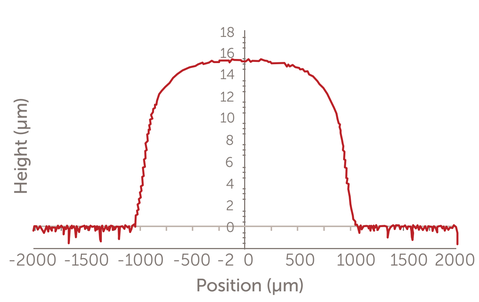
Embossed Polymer-based Wafer Contact Surface

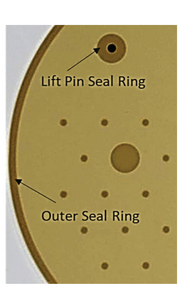
- Polymer is a high purity, low particle and pattern-able material.
- Compliant embossment system for minimal wafer sagging and backside damage under clamping force.
- Embossment height ranges from a few micron to hundred micron.



Embossed Plasma Etch-resistant Wafer Contact Surface

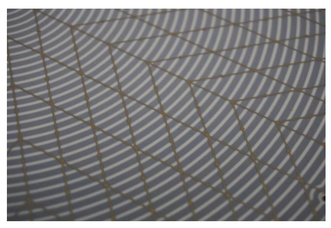
- Proprietary wafer contact surface solution best for e-chucks used in processes with plasma corrosion or erosion chemistry.
- Specialized physical mask system design to build an entire embossment system including seal rings in ONE deposition step rather than TWO.
- Mask design can also be customized to meet specific embossment pattern, density, and dimensional requirements.

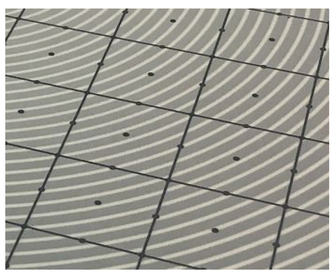




Embossed Electrically Conductive Wafer Contact Surface

- Wafer contact surface solution as the best meditation to reduce wafer sticking on e-chuck caused by residual surface charge.
- Various materials with different electrical conductivity available
  - — Metal nitride-based coatings (top)
  - — Carbon-base (bottom)
- Embossment system with engineered pattern can be fabricated by either PECVD or PVD, or combination of the two processes.
- Hard surface with excellent wear resistant performance.





SUMMARY

Entegris has extensive experience in developing e-chucks and tailoring embossed wafer contact surface material, structure, pattern and property to meet requirements of various operating environments. High purity hard and soft wafer contact surfaces with patterned embossment system can be fabricated by proprietary coating technologies and processes. E-chucks with specialized wafer contact surface have been field-proved in many semiconductor process applications such as ion implantation, plasma diffusion, dry etching, thin film deposition, metrology and wafer fusion bonding.