Zero Defects

Entegris Newsletter

October 2017

CONTENTS

Entegris Expands Its Taiwan Technology Center to Add New Microcontamination Analysis and Technology Development Capacity

Entegris announced on Sept. 12 the expansion of its Taiwan Technology Center for Research and Development (TTC) in Hsinchu, Taiwan. The expansion adds a new Microcontamination Control Lab (MCL) that focuses on filtration media development and is home to the company's relocated Asia Applications and Development Labs (AADL) for trace metal, organic contaminant, and nanoparticle analysis. This addition to the Center's existing R&D, formulation scale-up, and pilot production capabilities also creates a single, off-site collaboration location for our customers' specialty chemical, CMP and liquid filtration needs.

Key facts for the $8.5 million USD investment:

- Class 1000 cleanroom
- 5x increase in lab space
- Facility renovations and equipment upgrades

"Interactions and dependencies between process materials and equipment are at a critical evolution point as device scaling continues to be a leading driver for efficient construction of today's devices. Bringing the industry's brightest minds together in a state-of-the-art facility enhances Entegris' unique ability to meet these needs," offered Entegris Chief Operating Officer, Todd Edlund. *"By expanding the MCL facility, we bring together core-competencies in liquid filtration, specialty chemicals, and CMP to create more holistic analytical services and technology development solutions designed to meet our customer's Logic, DRAM, and 3D NAND device manufacturing challenges."*

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Reduced Defectivity Rates using Oktolex™ Membrane Technology in Photochemical Filtration Applications

By Lucia D'Urzo, Hareen Bayana, Aiwen Wu, Jad Jaber, James Hamzik - Entegris & Jelle Vandereyken, Philippe Foubert - imec

In July 2017, Entegris launched Oktolex™ membrane technology to improve yield in ArF, KrF, and EUV lithography for Logic, DRAM, and 3D NAND Devices. Each Oktolex membrane is tailored to target the specific defect-causing contaminants of each unique photoresist or photochemical.

Specific "killer-defects", such as micro-line-bridges are one of the key challenges in photolithography's advanced applications, such as multi-pattern. They generate from several sources and are very difficult to eliminate. Point-of-use filtration (POU) plays a crucial role on the mitigation, or elimination, of such defects.

The goal of this study is to provide a comprehensive assessment of Oktolex technology compared to other traditional photo-chemical membranes. Defectivity transferred in a 45 nm line 55 nm space (45L/55S) pattern, created through 193 nm immersion (193i) lithography with a positive tone chemically amplified resist (PT-CAR), has been evaluated on organic underlayer (UL) coated wafers. Lithography performance, such as critical dimensions (CD), line width roughness (LWR) and focus energy matrix (FEM) are also assessed.

SIEVING VS. NON-SIEVING PARTICLE REMOVAL

In sieving (size exclusion) removal, particles too large to pass though the pore structure of the membrane are captured either on the surface or in smaller passages inside of the structure. The smaller the pore size, the better the sieving efficiency will be.

Non-sieving removal is related to the adsorption of particles to the membrane surface and it is independent on the particle or pore size. A variety of intermolecular forces governs the interaction between the particle in solution and membrane surface such as electrostatic forces, Dipole forces, London forces, etc. As long as the particle can approach the membrane surface and experience a net attractive force, it will be captured.

The Oktolex membrane technology is an effective tool to improve membrane wetting properties, filtration efficiency and selectivity. The tailored membrane technology enables precise contaminant targeting without negative impact on the chemical composition.

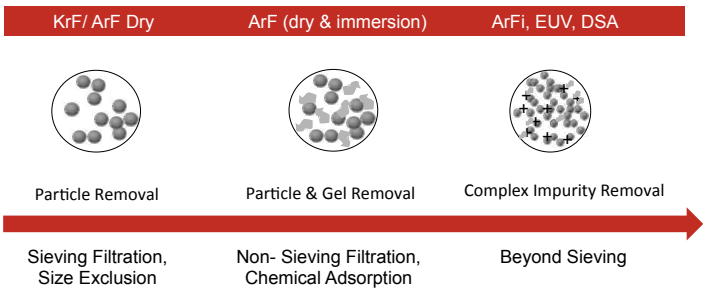

Figure 1. Illustration of different defect retention mechanisms.

EXPERIMENTAL

Equipment: lithography work was run in an ASML TWINSCAN™ NXT: 1970i with 1.35NA and a TEL® LITHIUS Pro-Zi track coat-develop system.

Material: the JSR PT-CAR AIM5484 coated on Brewer Science ARC®-29SR was used for patterned defect study.

Mask: a mask with solely L45P100 patterns and full field exposure was used for defectivity study.

Metrology: pattern wafers were inspected on KLA 2925. Defects were reviewed and classified on KLA eDR-7110. CD-SEM measurements were carried out on a Hitachi CG-4000 system.

Point-of-use-filtration: Oktolex and native ultra molecular weight polyethylene (UPE) were compared.

Defect library: defects were classified as in the defect library reported on Figure 2.

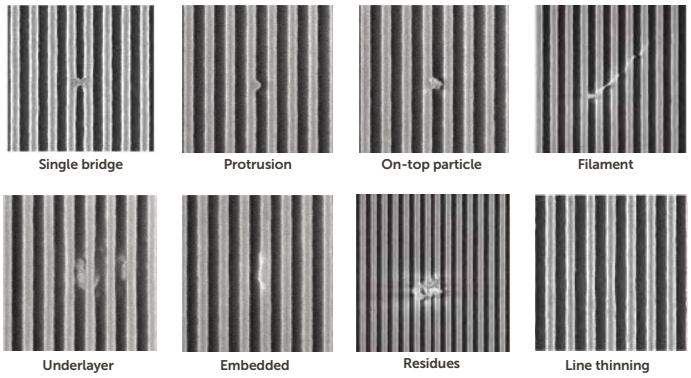

Figure 2. Defect library used in this work.

RESULTS

Defectivity

A typical defect pareto is shown in Figure 3. Each bar represents the normalized average of three wafers. For an easier comparison, data are normalized on aged resist results. The main defectivity mode related to resist filtration are micro-bridges and residues. Few filaments were also observed. On-top particles are mainly modulated by developer and rinse filtration, as reported elsewhere.[1] Defect from UL are not modulated by resist filtration
and are not object of this study. As we focus this research on resist filtration, both on-top and UL defects are removed from Figure 3 for clarity.

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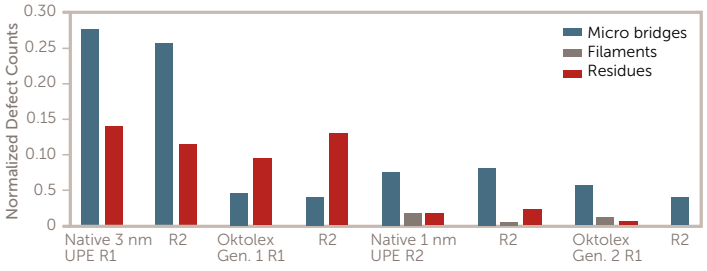

Figure 3. Normalized defect pareto.

While residues are clearly triggered by membrane pore size, micro-bridges are not. The normalized count of single bridge is reported in Figure 4. In the case of native membranes, the amount of micro-bridges is triggered by pore size shrinking. However, the Oktolex Gen. 2 filter performs similarly to native and Oktolex Gen. 1.

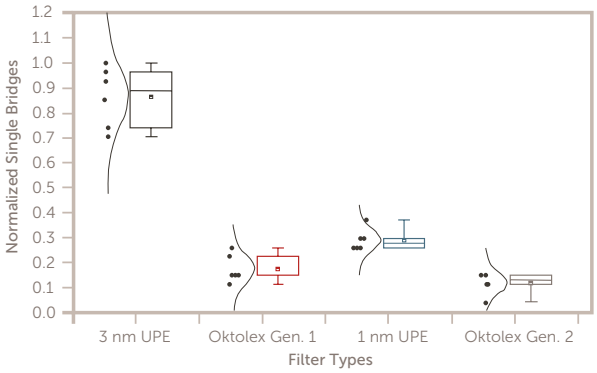

Figure 4. Normalized single bridge count/wafer, arranged by experimental group.

CD, LWR and FEM measurement

This study was complemented with CD, LWR and FEM measurements. CD and LWR results are shown in Figure 5 (a, b). Each point represent the average of 72 measurement locations/wafer. Apart a relatively broader distribution observed on 3 nm UPE, no significant shift between experimental groups has been measured.

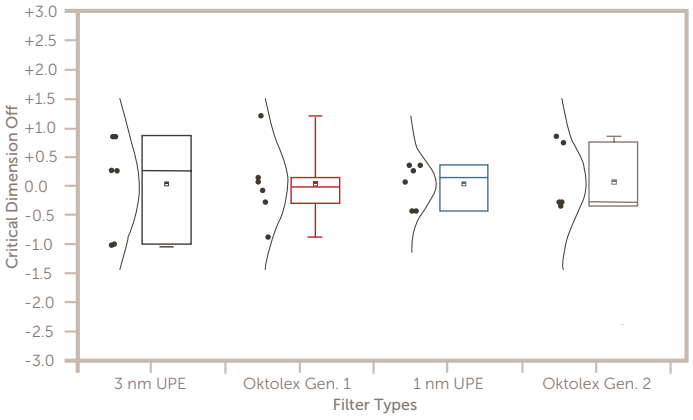

Figure 5a. CD offset calculated on 72 measurement locations/wafer. 3 nm UPE is taken as reference.

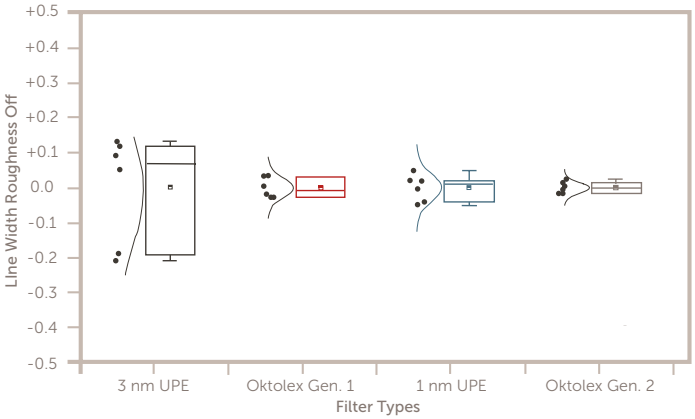

Figure 5b. LWR offset calculated on 72 measurement locations/wafer. 3 nm UPE is taken as reference.

FEM wafer maps are shown Figure 6, measured on 3 nm native UPE and Oktolex membrane. No changes have been observed between the two groups.

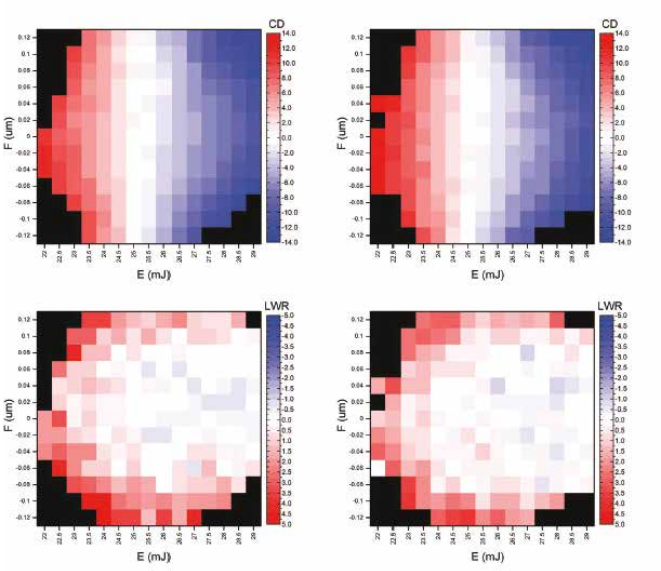

Figure 6. FEM wafers. The offset value for CD and LWR in the case of native (left) and Oktolex (right) are reported.

CONCLUSIONS

Oktolex membrane technology represents a powerful tool which enhances defect retention. In this work, **we demonstrated the superior performance of Oktolex, the best membrane technology in immersion lithography**. Even though Gen. 2 shows the best performance, an improved retention was achieved with Gen. 1. This allows a strong filter performance enhancement without necessarily shrinking membrane's pore size. It has been also proven that Oktolex membrane technology does not alter CDs, LWR and provides similar FEM, suggesting that no unwanted retention of resist components takes place.

Reference

[1] Kamei, Y., Shiozawa, T., Kawakami, S., Foubert, P., De Simone, D., D'Urzo, L., Bayana, H., Nafus, K., "Track process optimization for UV HVM," EUVL Symposium, Hiroshima, Japan (2016).

Metal Contaminant Reductions from Gas Streams

By Rocky Gipson, Ph.D., Manager of Gas Purification Research and Development - Entegris

Semiconductor device yields have long been impacted by device contamination. As process nodes continue to shrink from 10 nm to 7 nm and soon to 5 nm — pushing CMOS to its very limits — the sensitivity to metal contamination during manufacturing processes has increased significantly. This article describes the **primary causes of metal contamination in gas streams and ways to address the problem through the use of specially-designed gas delivery systems**.

WHERE DOES METAL CONTAMINATION ORIGINATE?

Possible root causes of semiconductor device contamination in the front- and back-end-of-line processes include cross-contamination induced by chemicals, ultrapure water and gases. The process environment, which includes the tools, network or gas/chemical distribution, and boxes for wafer handling and transportation, contribute to the problem.

Contaminants from the metallic components of process tools, plumbing and tubing play a role in metals contamination generation. Among the most common metallic contaminants are the transition metal constituents of 316L stainless steel — chromium (Cr), iron (Fe), manganese (Mn), molybdenum (Mo), and nickel (Ni) — as well as main group metals including sodium (Na), calcium (Ca), and aluminum (Al). Depending on the metal, it can degrade CMOS gate stacks, reduce carrier lifetime and more.

There are two main factors that contribute to metal impurities on a wafer due to the process environment itself:

1) metal contamination inherent to the gas supply; and

2) corrosion of metal surfaces induced by gases from the gas system itself due to the gases that are required by semiconductor manufacturing processes.

Not all processes requiring a gas supply use corrosive gases. Those that do, however, can impact the entire gas supply network. Dry etch processes, including ion beam etching, plasma etching, and reactive ion etching use corrosive gases that include arsenic pentafluoride, (AsF_5), boron trichloride (BCl_3), chlorine (Cl_2), hydrogen chloride (HCl), silicon tetrafluoride (SiF_4), and phosphine (PH_3), among others. Additional corrosives include dichlorosilane (SiH_2Cl_2, used in epitaxy) and chlorine trifluoride (ClF_3), which is used for cleaning various semiconductor tool components.

In a high-volume manufacturing environment, it is general practice to employ a main gas cabinet in the sub-fab environment to store the bulk gas supply for multiple process tools. The gas is delivered to individual tools using a valve manifold box. Because plasma etch and epitaxial tools can require the same corrosive gases, both are typically supplied from the same bulk source. This scenario subjects the entire gas delivery system to corrosion and contributes to the contamination of the gas supply itself.

Historically, the tolerance for metal contaminants in gas supplies was 10^{10} atoms/cm^2. As devices reach smaller nodes and sensitivity to contaminants increases, the industry has tightened purity standards 100-fold to 10^8 atoms/cm^2 in an effort to reduce defect-causing contaminants found in process gases. One way to meet this new standard is by using gas purifiers designed to remove moisture, hydrocarbons, and volatile metals from corrosive gasses and gas distribution systems, thereby reducing the release of metal contaminants to acceptable levels and subsequently improving wafer yields.

MITIGATING MOISTURE CONTAMINATION

High moisture levels in the corrosive gas stream are a significant contributor to corrosion. Mitigating moisture begins at the gas source and continues to the transportation and storage of the gas. If moisture can be reduced below a certain threshold (*ca.* 500 ppbV or greater), corrosion stops and volatile metals inherent to the gas supply can be removed.

Moisture contamination in gas supplies can reach hundreds of parts per billion (ppbV). By implementing a gas delivery system fitted with a mechanism that is designed to remove moisture from the supply, outlet concentration can be reduced to 15 ppbV or less.

REMOVING CONTAMINANTS FROM THE GAS SUPPLY

In addition to mitigating moisture, capturing volatile metal particulates using special filters diminishes the occurrence of wafer contamination.

While gas delivery systems themselves feature similar components, the process gases and the contaminants inherent to them vary from gas to gas. As a result, different gases may require advanced construction materials to remove contaminants. One solution to address this is incorporation of nickel filters in the purifier cartridge instead of stainless steel (see Fig. 1).

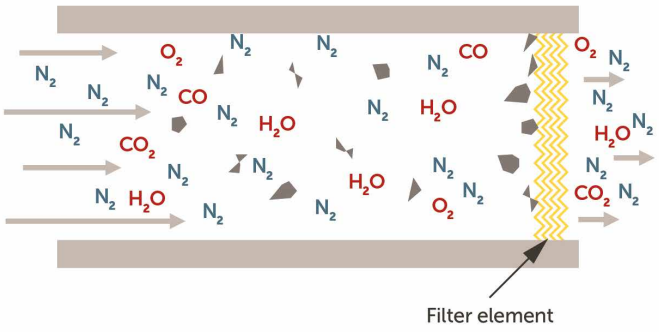

Figure 1. Filtration: A process or device that contains a porous element designed to prevent suspended solid particles from breaching the element barrier in a gas stream.

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Nickel provides a much greater degree of corrosion resistance, as it is virtually unreactive towards many corrosive gases. For best results, purifiers are installed at the gas source and at the tool (see Fig. 2).

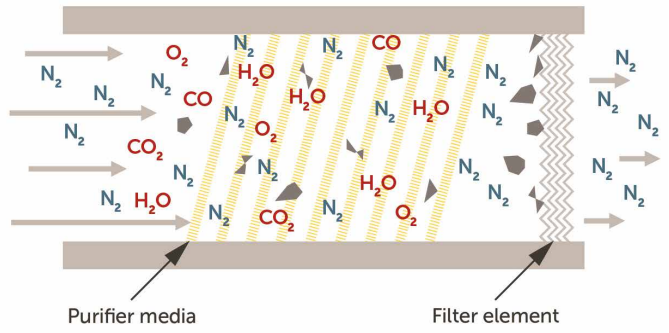

Figure 2. Purification: A process or device that contains media designed to "grab" molecular contaminants (O_2, H_2O, N_2, CO) as they pass through a gas stream using the principles of chemical adsorption.

CONCLUSION

Minimizing moisture in a gas supply to 15 ppb or below, combined with reducing on-wafer volatile metal contaminants to <10^8 atoms/cm² is the best strategy to improve final wafer yields, particularly in finer nodes. To achieve both these objectives, equipment such as Entegris' GateKeeper® GPU corrosive gas purifiers can be used. These point-of-use cartridges are con-structed using proprietary adsorbents combined with advanced corrosion-resistant particle filtration and are engineered to remove volatile metal contaminants and moisture from corrosive gas streams. The GPU family's moisture efficiency performance is validated using state-of-the-art analytical instrumentation. The purifiers can be mounted at the point of use and at the gas supply in any physical orientation to provide end users with flexibility when designing gas delivery systems.

The GateKeeper GPU family of gas purifiers.

SiGe Etch Selective to Ge for Ge Gate-All-Around Field Effect Transistors

By L. Witters, F. Sebaai, F. Holsteyns - imec, Leuven, Belgium and R. R. Lieten, S. Bilodeau, E. Cooper - Entegris

To continue the performance increase of CMOS-based integrated circuits for the N5 technology node and beyond, new device architectures are needed (see Fig. 1). Gate-all-around (GAA) field effect transistors (FETs) are promising candidates to replace finFETs (used for N22, N14 and N10) for future CMOS technology nodes (likely N5 and beyond).

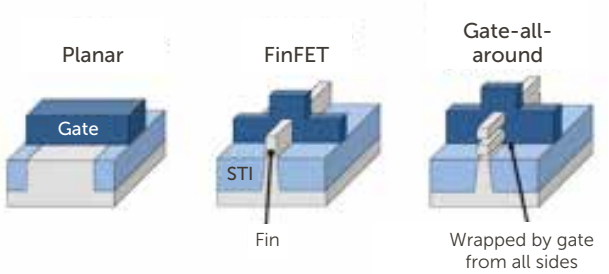

Figure 1. Evolution of device architectures: from planar FETs to FinFETs around N22 and likely from FinFET to GAA around (N5).

GAA FETs offer better electrostatic control (more gate interface area per channel volume) of the semiconductor channel than finFETs, and therefore enable further downscaling of the gate length, while maintaining low off current.[1] GAA technology enables a further decrease in device dimensions and hence an increase in performance per unit area (Moore's law). Horizontal GAA FETs are an evolutionary extension of the currently used FinFET technology, making this technology easier to implement than other technological options, like tunnel FETs or 2D materials. Finally, it is possible to vertically stack horizontal GAA devices, which allows a further increase in device density, and therefore increase in performance per unit area.

Besides changing the architecture of the transistor from fin to GAA, high mobility (relative to silicon) channel materials will be needed for N5 and beyond to increase the transistor speed. Thanks to its high hole and electron mobility, germanium (Ge) is a good candidate to replace Si as the channel material.

ENABLING THE FORMATION OF HORIZONTAL NANOWIRES CONSISTING OF Ge

To manufacture Ge GAA devices, it is important to be able to form Ge nanowires. In collaboration with the research institute imec, Entegris Inc. has developed a formulated chemistry that enables the formation of horizontal nanowires consisting of Ge.[2] This formulated chemistry (wet) etches SiGe alloys selectively to Ge. When starting from a SiGe/Ge/SiGe etched multistack Fin (see Fig. 2, left), exposure to this chemistry selectively removes the SiGe layers, leaving behind vertically stacked horizontal nanowires (see Fig. 2).

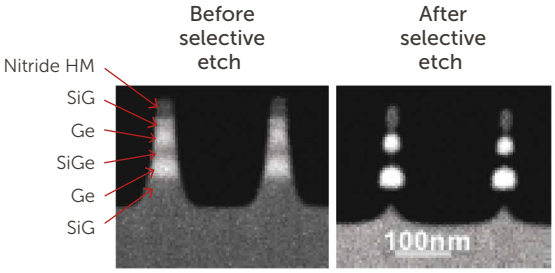

Figure 2. Cross section TEM image showing a SiGe/Ge multi stack before etching and released Ge nanowires after etching.[2]

Recently, imec has manufactured Ge GAA FETs with small gate length (40 nm) using this selective etch for Ge nanowire release.[3] In the following paragraph and Fig. 3, the details of manufacturing are summarized: a SiGe/Ge/SiGe multistack is grown lattice matched to a 300 mm (100) Si substrate. The SiGe layer consists of 55%–70% atomic Ge. Subsequently fins are etched with 45 nm pitch and isolated using shallow trench isolation (STI). To release the Ge nanowires, the sacrificial SiGe is selectively removed in the dummy gate cavity through wet processing. SiO_2/HfO_2 dielectrics and TiAl based workfunction metal is formed around the channel, with diameter of 9 nm.

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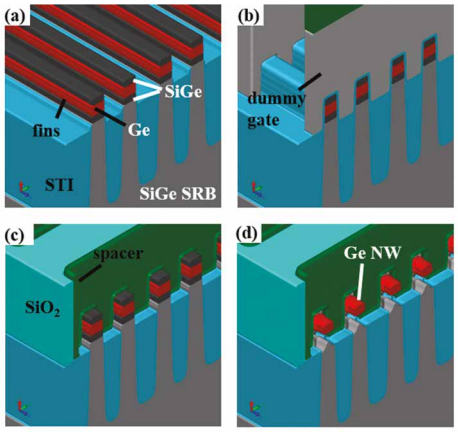


(100) $Si_{0.3}$ $Ge_{0.7}$ SRB virtual substrate

- Well + ground-plane implantation + anneal
- Epitaxial SiGe/strained Ge/SiGe deposition
- Spacer-defined fin patterning (SADP)
- Low temperature, low oxidizing STI and fin reveal **(a)**
- Dummy oxide + dummy gate patterning **(b)**
- B-extension implantation + SiN spacers
- Embedded B-doped SiGe S/D epi + SiO_2 dep + CMP
- Dummy gate and dummy oxide removal **(c)**
- Sacrificial SiGe layer etch **(d)**
- RMG: epi Si/SiO_2/HfO_2/WF metal/W fill metal local interconnect to S/D epi
- Interconnect 2
- Via + metal1
- Passivation

Figure 3. Process flow and Coventor® images (a) – (d) illustrating fabrication of strained Ge GAA NW devices starting from a 300 mm Siltronic® $Si_{0.3}Ge_{0.7}$ strain relaxed buffer (SRB) substrate using wet sacrificial SiGe removal to release the strained Ge wires inside the dummy gatecavity.[3]

The benefit of the GAA structure on electrostatics is obvious when comparing to finFETs: excellent drain induced barrier lowering (DIBL) and subthreshold slope saturation (SSSAT) values are measured down to the smallest patterned gates measured (LG = 40nm). The improved electrostatics for the LG = 40 nm devices are reflected in the ID-VG characteristics, where only the GAA devices can reach the high performance (HP) off-state current target of 100 nA/µm (Fig. 4).

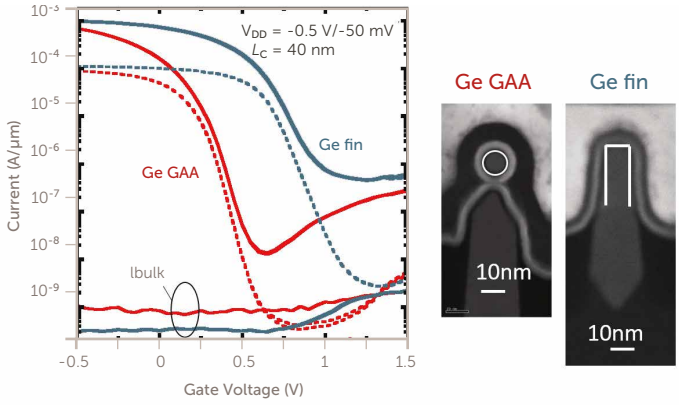


Figure 4. Short-channel (LG = 40 nm) drain–source and bulk current versus gate voltage for Ge GAA and Ge fin devices from.[4] All currents are normalized toward the effective channel width (30 nm for Ge GAA and 60 nm for Ge fin). Continuous lines at -0.5 V VDD and broken lines at -50 mV VDD.

CONCLUSIONS

Entegris has developed a wet, selective SiGe etch that enables the formation of horizontal Ge nanowires. Imec has applied this formulated chemistry to fabricate Ge GAA devices with short-channel (LG = 40 nm) and with a 9-nm diameter Ge NW on 300-mm (100) Si substrates with 45-nm dense pitch. Compared to strained Ge finFETs, the devices show significantly improved short-channel control with drain-induced barrier lowering (DIBL) of 30 mV/V. A record-breaking SSSAT of 76 mV/dec was achieved for LG = 40-nm Ge channel pMOSFET devices and OFF-state current of 3 nA/µm.

References

[1] Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates, H. Mertens et al., VLSI 2016.

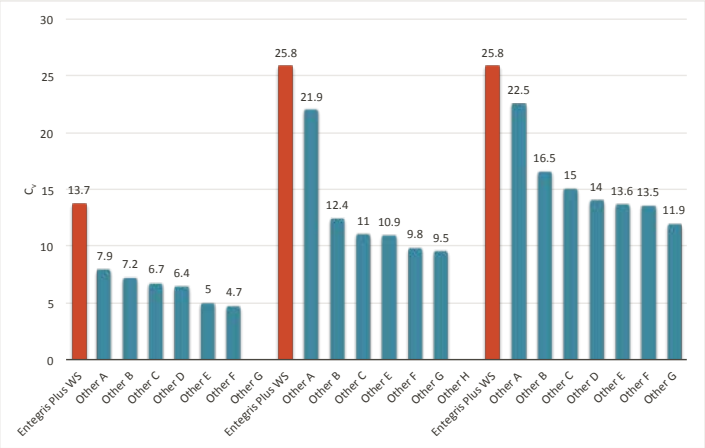
[2] Wet Selective SiGe Etch to Enable Ge Nanowire Formation, Farid Sebaai et al., Solid State Phenomena 255, pp 3-7.

[3] Strained Germanium Gate-All-Around PMOS device demonstration using Selective Wire Release Etch prior to Replacement Metal Gate Deposition, L. Witters et al. VLSI 2017.

[4] J. Mitard et al., "A 2nd generation of 14/16 nm-node compatible strained-Ge pFINFET with improved performance with respect to advanced Si-channel FinFETs," in Symp. VLSI Technol. Tech. Dig., Jun. 2016, pp. 34–35.

New Integra® Plus Weir Style (WS) Fluid Management Valves: The Solution for High Flow Corrosive Chemicals Used in Semiconductor Manufacturing Applications

The new Integra Plus WS valve utilizes a streamlined fluid flow path for improved flow performance. Flow-rate testing on the new valves has yielded the following results, when compared to alternative valve solutions:



The new valves offer an **innovative, single-piece and adhesive-free diaphragm design** that directly couples the diaphragm to the valve actuator to **eliminate potential diaphragm separation** in vacuum applications and **increase valve life**. They are constructed from high-purity, chemically resistant PFA and PTFE to **maintain chemical purity** and features a **small footprint** to reduce required space within equipment.

Integra Plus WS valves are available with PrimeLock®, Flaretek® and PureBond® pipe port connections. Unique configurations with PrimeLock or Flaretek on one port and PureBond pipe on the other port provide system flexibility, space reduction and easy installation into any fluid handling system.

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