96 Layers and Beyond:

Solving 3D NAND Material and Integration Challenges

White paper

INTRODUCTION

We have reached an era in which a wide variety of computing applications are demanding a doubling of digital storage capacity every 1.5 years. Social media, video and photograph storage, memory sticks, storage centers, and data analytics are putting pressure on chip manufacturers to increase memory density. Demand fuels innovation, and the shift from 2D to 3D NAND storage is a clear example.

Multiple types of memory are available to satisfy various market demands. The memory pyramid (Figure 1) illustrates this well. At the top of the pyramid, the applications require fast embedded devices, while at the bottom the requirements demand less speed but require low cost. NAND memory resides in the middle below DRAM. In terms of requirements, NAND stands alone —it needs to be quite fast, but also low cost. The NAND architecture, which is read in strings of cells rather than individual cells, is most useful when storing large amounts of data such as video, photographs, and documents.

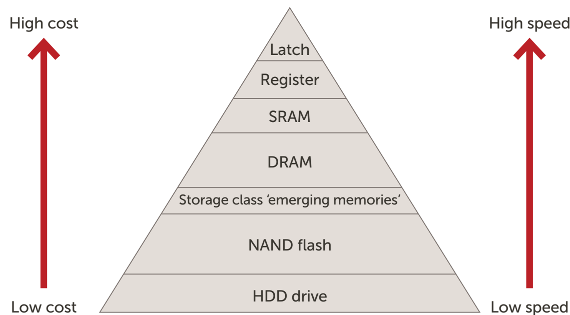


Figure 1. The memory pyramid.

In the same way that population density is greater in high-rise buildings than in single story houses, the pressure to increase the number of bits stored in a given area resulted in a shift from 2D to 3D NAND storage during the past decade. From a device fabrication point of view, this replaced the challenges of shrinking device dimensions with stacking challenges (Table 1). The transition to 3D NAND also allowed an important added benefit, which is the Gate All Around (GAA) geometry. This helps with the fundamental issue of shrinking gate size—running out of material to store sufficient charge. This paper highlights some of the new stacking related challenges and proposes solutions to allow designers to increase the number of layers in 3D NAND structures to 96 and beyond.

2D (planar cell) major challenges	3D (GAA) major challenges
Advanced lithography (technically and cost)	High aspect ratio etching (profile control, mask formation, and selectivity, etc.)
Not enough charge available to store multiple bits	High aspect ratio deposition (uniformity and quality in extreme geometries)
Cross talk between cells	Need to access cells in 3D (staircase structure required)
Uniformity of cell performance	–

Table 1. Challenges of 2D versus 3D NAND Structures.

SCALING CHALLENGES

When scaling 3D NAND, moving beyond 96 layers to 128 and higher seems to be the breaking point where changes in materials and fabrication processes will be necessary to maintain yield and performance at an acceptable level. The high aspect ratio (HAR) of these devices poses two primary types of challenges:

- Achieving uniform material properties from the bottom to the top of the stack
- Keeping contamination low to avoid yield loss as the structure is built up

The uniformity challenge affects several aspects of the 3D NAND structure. If the composition and electrical properties of the silicon oxide (SiO_2) and silicon nitride (Si_3N_4) layers vary from the bottom to the top, the device will not function as designed. Under- or over-etching of the nitride layers is another yield-loss risk that becomes greater as the layers increase. Deposition and etch processes, therefore, need to be optimized for these HAR structures.

The more layers a 3D NAND device has, the more its performance can be constrained by electron mobility in the vertical silicon channel. As explained in the paper "Considerations for Improving 3D NAND Performance, Reliability, and Yield," doping the silicon with germanium (Ge) increases electron mobility. The challenge, however, is achieving uniform distribution of Ge throughout the channel.

Film purity is becoming increasingly more critical in a working device. As device structures become thinner and narrower with each device node, there is less space for thin films. Making these high-integrity thin films requires high-purity materials, which calls for minimizing the presence of trace impurities.

Keeping contamination as low as possible applies to all aspects of 3D NAND fabrication. Device structures are more susceptible to damage from even smaller particles, and the number of layers in 3D NAND makes the contamination problem cumulative. Steps to improve film purity and reduce contamination extends to choices in materials, coating and etching processes, and equipment used in the various process steps.

Scaling to ever increasing number of cell layers and beyond will have to involve a string stacking approach, with multiple vertical memory structures built on top of one another. Each structure, however, will contain at least 64 layers and perhaps 96. Moreover, high-volume manufacturing solutions that will work with 100-layer structures and challenging aspect ratios of around 100:1 still need to be developed. Fortunately, many such solutions have demonstrated proof of concept, and some are ready for full-scale implementation.

DEPOSITING CONFORMAL COATINGS

The HARs in 3D NAND devices create challenges for thin-film deposition processes. Plasma-enhanced deposition processes, which are effective for the initial SiO_2 and Si_3N_4 layers in a device, are not suitable for the complex topographical features that are present in the 3D NAND stack. The most extreme geometry in the 3D NAND structure occurs when depositing cell layers such as aluminum oxide (Al_2O_3). These layers need to pass through the vertical slot, along a lateral slot, then around the cell's GAA structure. Although it is possible to conformally coat sections of the structures using a plasma-enhanced process, the properties of the deposited films will likely vary from the bottom to the top of the structure. In many cases, the properties of the film deposited on the vertical side walls are quite different from those of the film deposited on top of the structure. This inherent nonuniformity of the plasma process can create unacceptable variations in chemical composition, film density, and electrical properties within the device structure. For these reasons, plasma-enhanced processes do not work well for HAR features.

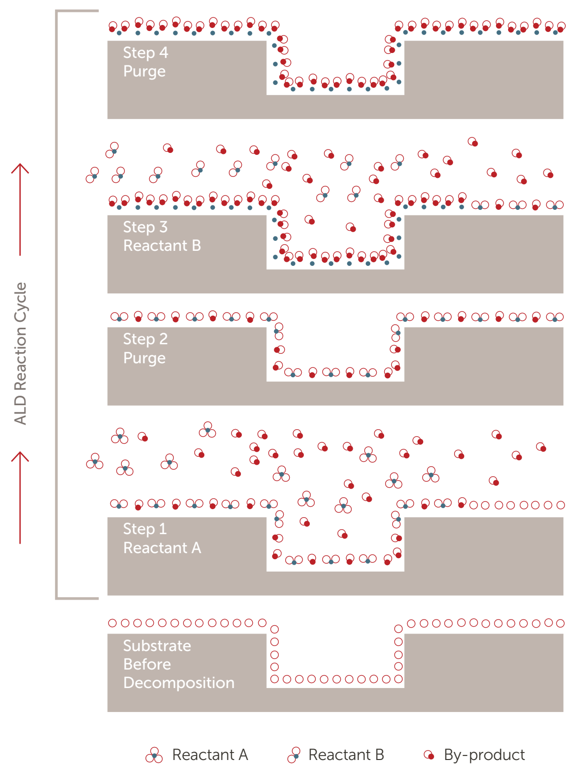
Thermal atomic layer deposition (ALD) is a much better way to achieve uniform layer deposition throughout all the dozens of layers in a complex 3D NAND structure. Although the ALD process is often considered 'slow' for manufacturing processes, the control of the film's composition, conformality, and morphology can override the concerns of manufacturing speed.

In the ALD process, a precursor is introduced into the system to coat the 3D structure uniformly, regardless of topography. This precursor may be in the form of a gas, a liquid, or a solid, with a trend toward increasing adoption of solid precursors. The precursor is purged with inert gas and a second co-reactant is added to the system. The co-reactant is then purged to complete the cycle. The ALD process requires multiple cycles to uniformly build up the desired thickness of the deposited film. A schematic representation of a single cycle is shown in Figure 2.

Reacting two or more species in a pulsed manner allows the film to grow monolayer by monolayer. Surface reactions, rather than mass transport, control the deposition process. By controlling the reactant dosing sequence, ALD can coat a complex 3D vertical structure uniformly, regardless of the surface complexity. The reaction by-products are transported away from the growing film surface during the purge steps. Therefore, the film remains highly uniform and conformal throughout the entire thickness of the 3D NAND structure. ALD methods can be extended to a greater number of layers to meet future device node specifications.

As an alternative to thermal ALD, it is possible to modify a more conventional chemical vapor deposition (CVD) thin-film process so that it conveys some of the advantages of ALD. In this case, the precursor and the co-reactant are pulsed in a cyclic sequence rather than being reacted at a constant rate throughout the process. Pulsing during CVD creates a thin-film deposition process that is limited by surface reaction kinetics, a regime that is well-suited to depositing conformal thin-film coatings. The pulsed CVD approach can result in good thin-film conformality over complex topographical features and 3D geometries.

In some cases, films grown using the pulsed CVD process are identical to those grown with ALD in their conformal coating ability, film purity, and resulting thin-film device performance. For these films, pulsed CVD provides a lower-cost option for facilities that do not have ALD tools readily available.



Reference: Taken from H. Oomine, MS Thesis, Tokyo Institute of Technology.

Figure 2. Schematic representation of an ALD process.

PRECURSOR SELECTION AND THE PROBLEM WITH CARBON

Whether depositing with ALD or pulsed CVD, the choice of a precursor is critical to the success of the process. The necessary precursor requirements include high molecular purity, high elemental purity, a useful vapor pressure under normal operation conditions, thermal stability at the operating temperature for extended time periods, and the ability to deposit conformal films with the desired electrical properties. Additionally, metal precursors must deposit films that display sufficiently low electrical resistivity.

Of the listed precursor requirements, purity is increasingly important with each successive device node, making contamination a serious issue. Carbon contamination is of special concern since its presence can degrade electrical performance over the lifetime of the working device. Organometallic precursors, which contain carbon ligands, often leave some small amount of carbon in the deposited film. Inorganic precursors, on the other hand, contain no carbon ligands and thus enable carbon-free films.

High-purity, inorganic precursors are therefore preferred for 3D NAND devices. The challenge with many inorganic precursor materials is that they tend to be solids under typical operating conditions. Solid precursors require special solid delivery ampoules and highly controlled, uniform heating of delivery lines and reactor components to prevent solid condensation. Uniform heating is critical for achieving uniform precursor delivery and uniform film growth across 300mm wafers, as required for full-scale manufacturing processes.

SILICON NITRIDE WET ETCH SELECTIVITY

Selective wet etching of the Si_3N_4 layers in 3D NAND devices is reaching a ceiling for structures around 100 layers thick. Standard selectivity calculations based on results from blanket nitride and oxide wafers do not translate well to the complex structure of a 96-layer 3D NAND device. As a result, specially formulated chemistries are needed. A new approach is being developed that will yield selectivity data that correlates with expected results in real 3D structures. It should be possible to use this new approach to create a phosphoric acid-based chemistry that contains the optimum mix of additives to improve selective etching of Si_3N_4 throughout all the device layers.

Even with specially formulated chemistries, wet etch remains a time-consuming, expensive process. The extreme geometries of 3D NAND lead to a very narrow process window. Unlike for structures with more planar geometries, adjusting the silicon concentration in the bath is not sufficient. The silicon concentration increases exponentially with the depth in HAR features. The excessive silicon concentration in the feature will cause undesired selectivity, with silicon dioxide redepositing back onto the oxide surface and causing pinch-off in the bottom of the feature. Additives can mitigate this silicon concentration gradient and enable more uniform and selective nitride etching. The wider process window decreases etching time and chemical waste, thereby saving cost.

CMP CHEMISTRY AND EQUIPMENT

Chemical mechanical planarization (CMP) is used extensively in the 3D NAND fabrication process. It is both a critical and an expensive step that needs to be done properly to prepare surfaces for the next layer of metals and dielectrics while not accidentally contributing to yield loss. Changes in slurry chemistry, cleaning chemistry, pads, conditioners, and brushes are needed to alleviate some of the contamination and performance challenges that are unique to 3D NAND.

Slurry chemistries are changing to meet the goals of reducing the etch rate of metal layers and improving etch selectivity. The stabilizers added to slurries to achieve these goals contain trace metals which, if not thoroughly removed, can transfer to the wafer surface and cause electrical shorts.

The post-CMP cleaning step is especially critical because of the combination of materials used in the 3D NAND structure. Commodity cleaning chemistries (cleans) are no longer sufficient when faced with multiple layers of tungsten over Si_3N_4. The trace metals, especially iron (Fe), that are present in CMP slurries cause unacceptable yield loss if they are not thoroughly removed, and commodity cleans cannot remove enough of the iron. Commodity cleans can also cause over-etching of the tungsten layers, which is another potential source of yield loss.

The next generation of 3D NAND devices demands specially formulated cleans custom-designed to work with a specific slurry chemistry. When optimized properly, formulated cleans can remove trace metal contaminants effectively while minimizing etching of tungsten metallization. The ideal formulated clean is tailored to the specific materials used in 3D NAND devices while also being environmentally friendly.

The brushes used for post-CMP cleaning produce another source of potential contamination. One way to remove any trace metal content in the brushes is to ensure they are precleaned with chelating solutions before they are shipped to device manufacturers. Modification of the brush surface can also help by increasing the zeta potential of the brush so it won't accumulate particles during use. Surface modification reduces the possibility that unwanted trace contaminants transfer from the brush to the wafer during cleaning.

Brushes are commonly shipped in preservatives, such as hydrogen peroxide or ammonium hydroxide, to protect them from microbial growth during shipping and storage, and to extend their shelf life. This benefit, however, comes with the drawback of increasing the risk of contamination from impurities in the chemical preservatives. Therefore, as critical dimensions decrease, device manufacturers often prefer brushes shipped in pure deionized water and are willing to sacrifice their shelf life to avoid the potential yield loss caused by nanometer-size particles.

As new CMP pads are developed to meet the challenges of 3D NAND geometries, new conditioners must also be developed. Diamond grits are not sufficiently stable because of their non-uniform wear when used for this application. Graphite-based CVD conditioners, diamond-like materials grown with CVD, are proving to be more stable and longer lasting. The material cost of CVD conditioners is higher than that of conventional conditioners, but the increased lifespan more than makes up for the additional cost because of the dual benefits of lower chemical consumption and less equipment downtime.

Formulated cleans optimize surface repulsion and metal removal, modify particle surfaces, and create negative surface charges.

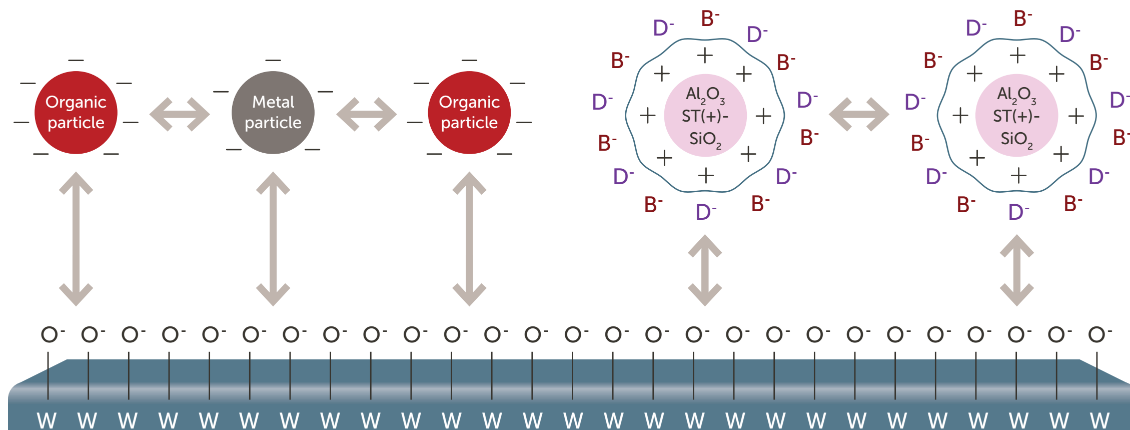


Figure 3. Schematic representation of formulated cleans removing particles and trace metal residues without metal etching.

CONTAMINATION AND MATERIAL PURITY

The large number of plasma etch steps required for 3D NAND puts additional demands not only on the etching process itself but on the components in the chambers in which the wafers are etched (Figure 4). Chamber components are typically coated with metal oxides to protect them from plasma attack and corrosive chemicals inside the etch chambers. Plasma spray coating with yttrium oxide has been the industry-standard process for decades, but this method is becoming problematic for two reasons: coating integrity and coating coverage.

First, plasma spraying creates a relatively porous, rough coating. The complex structures of 3D NAND devices are more susceptible to failure by contamination due to erosion of plasma spray coatings because of the extensive etching time and high temperatures required for 3D NAND processing. When the spray coating degrades, particles from the coating are deposited on the wafers and create unacceptable contamination levels.

Second, spray coating is best suited to planar surfaces due to inherent limitations of the coating process. Deposition and etch tools used for 3D NAND processes are built using parts that have complex shapes, which can't be coated sufficiently with plasma spray. Unless all surfaces of the component are coated with an even layer of oxide, the component cannot be adequately protected from corrosion during plasma etching.

The solution lies in borrowing processes from semiconductor fabrication. Physical vapor deposition (PVD) of yttrium oxide creates a uniform, dense conformal coating. Scaling up the PVD process to industrial-scale equipment built specifically for this purpose enables protective coatings for a variety of etch chamber parts. The ability to articulate the source and the part in three dimensions during PVD allows the tool to conformally coat all the surfaces of complex shapes, even though PVD normally requires a line of sight.

The most critical etch chamber components are those closest to the wafer, but the industrial scale of the tailored PVD process allows coating of most chamber components. Starting with an ultra-high-purity, PVD target creates a high-purity coating, minimizing the risk of contaminating the wafer with foreign particles.

The many deposition steps required for 3D NAND fabrication also rely on maintaining a consistent and repeatable physical state of the chamber and chamber components for process repeatability. Some of the chemistries used in deposition chambers cause corrosion or component oxidation, leading to changes in the physical state of the chamber and causing the process to drift.

Deposition chamber parts such as gas distribution components have intricate geometries or HAR features, which are extremely hard to protect from corrosion. Gas showerheads contain thousands of small holes that PVD coatings cannot reach. Corrosive chemistries are delivered through these showerheads directly to the wafer, making component integrity and cleanliness especially important.

Because PVD coating is not suitable for HAR features, gas distribution components demand a different coating method. The solution is to use ALD to deposit yttrium or aluminum oxides and create a uniform protective barrier. With ALD, high-purity coatings that are nearly defect-free can be deposited on every surface of complex chamber parts, including those with narrow or deep HAR features. Scaling of the ALD process to industrial scale allows the 3D deposition chamber components to be protectively sealed, leading to improved process stability for 3D NAND fabrication (Figure 4).

Parts shaded in gray are examples of various coated components in a typical deposition or etch chamber.

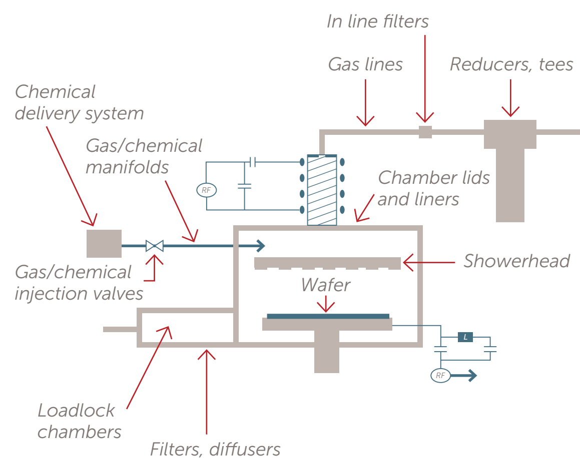


Figure 4. Scaling-up ALD allows for conformal, defect-free, high-purity coating of complex etch and plasma chamber parts for reduction in particle contamination, corrosion resistance and better process stability.

IMPROVING HARD MASK MATERIALS

Transferring lithographic patterns onto multi-layered device structures requires a hard mask in combination with an aggressive plasma-etch chemistry. The chemical composition and durability of the hard mask are key to a high-integrity pattern transfer process. If the hard mask degrades during the etching process, loss of the pattern or loss of a vertical profile will cause device yield issues.

Typically, the hard mask composition is tailored to the specific plasma-etch chemistry to provide the highest level of pattern transfer. As the number of layers in a device increases at advanced device nodes, the requirements and demands on the hard mask are also increasing. The hard mask must endure the harsh plasma etching environment for a longer time because of the greater number of layers being etched.

Hard masks may consist of thick amorphous carbon films or a wide variety of other similar materials that can withstand the plasma etching process. Amorphous carbon is an imperfect hard mask material for 3D NAND applications because it is susceptible to etching when exposed to the reactive plasma for the length of time required to process 3D NAND structure. Two methods for increasing the lifetime and etch durability of amorphous carbon are being considered: 1) doping the carbon layer with other etch-resistant elements, such as boron or 2) depositing a thin metal or metal oxide layer on top of the carbon mask layer. Both approaches are likely to have some merit but require either adding an extra processing step or modifying existing process steps.

Boron is available in solid, liquid, or gaseous form. A solid must be vaporized to incorporate it into the carbon layer, which adds complexity to the doping process, when compared to a liquid or gaseous species. Boron in liquid form can be highly reactive, causing an unacceptable safety hazard. Plasma-enhanced chemical vapor deposition (PECVD) from diborane is, therefore, the most reasonable approach for supplying boron and driving it into the amorphous carbon layer. It is cost-effective because it takes advantage of an existing gas delivery system, is already used in the industry, and may be safer than more reactive boron sources.

Doping amorphous carbon with boron hardens the material, forming boron carbide and making the hard mask resemble a ceramic. The risk is that boron may be too effective in increasing the etch resistance of the hard mask. The hard mask eventually needs to be stripped using reactive ion etching (RIE), and incomplete removal can cause as much of a problem as premature etching of the hard mask. The challenge is to add just the right amount of boron to increase etch durability. The PECVD process for boron incorporation will require extensive testing to optimize it before it is ready for commercial use.

Instead of improving the etch-resistance of the amorphous carbon itself, the second method for improving the hard mask adds an extra layer of protection. A variety of metal oxides— zirconium oxide (ZrO_2), yttrium oxide (Y_2O_3), Al_2O_3, and others—can be deposited at relatively low temperatures (400°C) via ALD, CVD, or PVD processes. The choice of metal oxide film may depend upon the etch chemistry chosen for the pattern transfer process. For example, Y_2O_3 films might be advantageous to use with fluorinating plasma etch chemistries, resulting in relatively stable yttrium fluoride (YF_3) surfaces during etching. Similarly, alternating metal oxide layers may be another way to ensure excellent plasma etch durability and high-integrity pattern transfer. Alternatively, the metal oxide etch layer could simply replace the hard carbon layer completely and eliminate any extra processing steps.

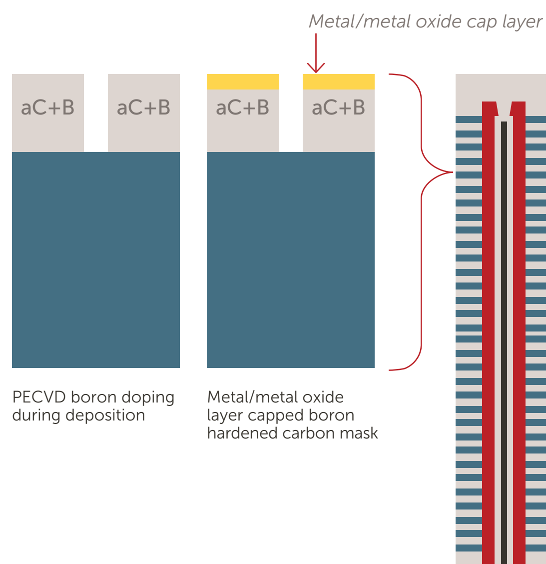
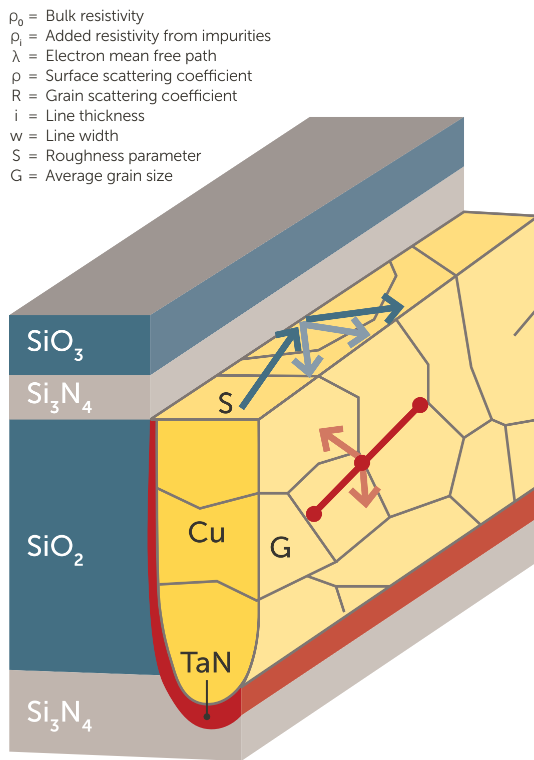


Figure 5. Two methods for increasing the plasma resistance of the amorphous carbon hard mask. (1) Implanting boron, (2) Adding a hard metal oxide layer.

While adding a layer on top of the amorphous carbon does improve its etch resistance, this approach requires the additional steps of depositing the metal or metal oxide layer and etching it away. Depositing multiple alternating layers complicates the hard mask process further, so it is important to weigh the total cost of ownership versus device performance enhancement before deciding whether to implement this method of improving hard mask etch resistance.

As device dimensions continue to shrink, the conductor line dimensions must also shrink. Similarly, the volume available for metal in inter-level vias is decreasing, which can result in increased via resistance. The electrical resistivity increases dramatically for films below 50 Å in thickness; a result of defect scattering and roughness within the metal films. Studies on copper (Cu) metallization have shown that the measured film resistivity is a function of the bulk metal resistivity (ρ), the film purity, film defects, film grain size, the electron free-mean path (λ), and surface scattering effects resulting from film roughness, as shown in Figure 6.



Reference: Recreated from M. O. Bloomfield and T. S. Cale, Advanced Metallization Conference Proceedings, XIX, 2004 p. 233; G. Schindler, M. A. Meyer, G. Steinlesberger, M. Engelhardt, and E. Zschech, Advanced Metallization Conference Proceedings, XIX, 2004 p. 205.

Figure 6. Cross-sectional schematic view of a Cu via used to demonstrate the various influences and variables on the measured film resistivity.

Film resistivity, which is a sum of contributions from bulk resistivity (ρ_0) and resistivity from impurities (ρ_i), is calculated as shown in Equation 1. In the equation below, ρ is the surface scattering coefficient, R is the grain boundary scattering coefficient, t is film thickness, w is line width, S is a roughness parameter, and G is average grain size.

$$\rho=(\rho_0+\rho_i)\left[1+\frac{3}{8}(1-\rho)\,\lambda\left(\frac{1}{t}+\frac{1}{w}\right)\cdot S+\frac{3}{2}\left(\frac{R}{1-R}\right)\frac{\lambda}{G}\right]$$

Figure 7 demonstrates the interplay of these combined effects on the total film resistivity, showing the multiple factors that cause resistivity to increase suddenly as interconnect lines become narrower. The significant increase in resistivity appears when dimensions shrink to nanometer-scale. The grain size effects dominate when the grain size is no larger than the thickness of the film. High-temperature annealing can increase the film grain size and decrease film defects, but the resistivity of a nanometer-scale film remains higher than that of a bulk Cu film (Figures 7 and 8).

Contributions to Total Resistivity (Representative)

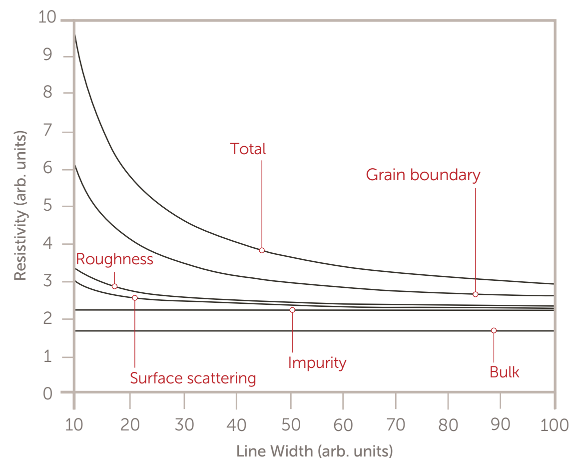


Figure 7. Plot showing the contribution of impurities, surface scattering, film roughness, and grain boundary defects to film resistivity as a function of line width.

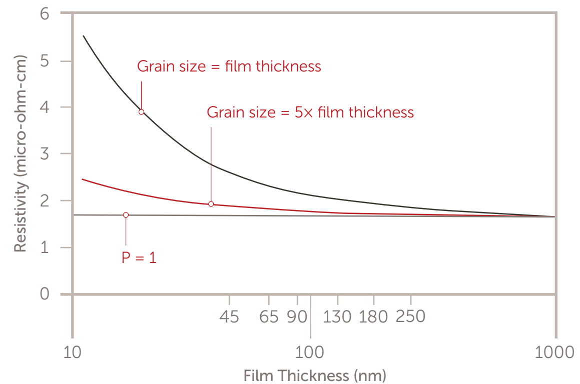


Figure 8. Plot demonstrating the impact of grain size on the resulting Cu film resistivity. Taken from S. M. Rossnagel and T. S. Kuan, J. Vac. Sci. Tech. B22 (1), 240 (2004). W. Steinhogl, G. Schindler, G. Steinlesberger, and M. Englehardt, Phys. Rev., B 66 075414 (2002).

CONSIDERING ALTERNATIVE METALS

The above studies investigated Cu lines, but the results are equally applicable to multiple metals that may be used as conductors in semiconductor devices. Tungsten, chosen for its low resistivity and minimal electromigration, has long been used for metal interconnects and contacts in 3D NAND. For future device nodes, however, alternative metals with lower thin film resistivity or other beneficial properties are being considered. Some alternative metals with higher bulk resistivity values may actually be preferable when used in very thin, narrow HAR films.

Metals under consideration include cobalt (Co), ruthenium (Ru), iridium (Ir), and molybdenum (Mo). No one metal is perfect — those with the best electrical properties come with other drawbacks — but, if integration challenges can be overcome, some of these alternative metals may find use in 3D NAND structures. Table 2 compares the advantages and disadvantages of various metals.

ALTERNATIVE METAL	ADVANTAGES	DISADVANTAGES
Co	• Abundant and low cost • Seamless via fill possible • Selective deposition known	• Corrosion issues leading to device integration challenges
Ru	• Good electrical properties • Conducting oxide, RuO_2	• Fluctuating cost • Corrosion issues • CMP integration challenges • Highly toxic RuO_4
Ir	• Excellent electrical properties • Conducting oxide, IrO_2	• Lack of natural abundance • Expensive • Best suited to specialty device applications (i.e., FeRAM)
Mo	• Abundant and low cost • Good electrical properties • Should be easy to integrate	• Not currently used in memory or logic • Need to demonstrate integration

Table 2. Comparison of potential alternative metallization for 3D NAND structures.

The interest in alternative metals is driving research into possible CVD and ALD precursors for these metals. New precursors need to perform as well as the existing precursors for tungsten while being cost effective. The trend toward creating custom-designed precursor molecules dovetails well with the effort to replace tungsten. The new precursors will need to be carbon-free, but the exact chemistries have yet to be developed.

TOWARD FLUORINE-FREE TUNGSTEN

One of the problems with tungsten centers around the use of tungsten hexafluoride (WF_6) precursor to deposit it. The presence of fluoride can release free fluorine (F), an especially reactive species that increases contact resistance. The presence of F has not been a problem historically, so the low cost and well-developed processes of the WF_6 precursor have outweighed any concerns about its effect on performance. For future device nodes, however, the barrier layers are so thin, that attack from fluorine will cause significant yield loss. Device testing has already shown degradation of the metal layers when fluorine interacts with titanium nitride (TiN). At some point, device performance will tip in favor of a fluorine-free tungsten (FFW) precursor.

Tungsten pentachloride (WCl_5) is a potential substitute for WF_6, but it has not been adopted in high volume because of its relatively high cost. It may be more economically feasible to use WCl_5 as a precursor for the initial nucleation layer of tungsten over TiN and then revert to WF_6 for the remaining film thickness. Adding WCl_5 to a single layer may provide sufficient protection for the TiN while not substantially increasing manufacturing costs.

SUMMARY

The challenges inherent in scaling 3D NAND to 96 layers and beyond impact all phases of device fabrication and the tools and materials used to fabricate the devices. The semiconductor industry needs to rethink decades-old practices that are no longer as effective in extremely HAR structures. It's generally understood that changing the chemistries used in deposition and etching steps sometimes means switching to more expensive materials, but improvements in yield allow the total cost to stay competitive. The same is true for the metal layers within the 3D NAND structures.

Contamination and material purity become more important than ever as device scaling continues. The effort to minimize contamination includes steps such as pre-cleaning CMP brushes or changing how etch and deposition chamber tools are coated. Making these changes successfully will require cooperation throughout the supply chain from material and chemical suppliers, component suppliers, equipment manufacturers, and semiconductor device manufacturers. In the long run, improvements in materials and process integration will enable high-yielding 3D NAND structures to support the ever-increasing device storage needs.

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References

[1] "Considerations for Improving 3D NAND Performance, Reliability, and Yield," Entegris White Paper, March 2018.

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