ZERO DEFECTS

Entegris Newsletter

March 2016

CONTENTS

1. Entegris News

- Entegris Expands Analytical and R&D Operations for Semiconductor Process Liquid Filtration in South Korea
- SPIE Advanced Lithography

2. Cost Reduction

 Improved Ion Implant Exhaust Management Reduces Energy, Capital Costs

3. Innovation

- CVD Cobalt Selective Deposition for Bottom-up, Void-free Via Fill
- An Update on Pellicle-compatible EUV Inner Pod Development

7. Product Highlight

FlowPlane™ Linear Filtration
 Technology: Enabling Nextgeneration Cleanliness and
 Contamination Control
 Performance in Advanced
 Technology Node Applications

Entegris Expands Analytical and R&D Operations for Semiconductor Process Liquid Filtration in South Korea

New capabilities help optimize filtration for specially formulated chemistries

Entegris announced the expansion of its liquid filtration/purification analytical science and research and development facility in Suwon, South Korea. As an addition to its existing Korea Technology Center (KTC) facility, the expanded lab includes advanced chemical/water analysis and material characterization capabilities, along with filtration device instrumentation. These new capabilities will allow closer collaboration with local customers to solve specific liquid filtration challenges by providing optimized solutions for their advanced processes.

"Sophisticated analysis of the interaction and compatibility between complex process chemistries and filtration devices is increasingly important as technology nodes advance. We continue to invest in these technologies — close to our customers — to optimize the performance of our filters with the unique chemical solutions our customers

require," said Entegris Vice President of Liquid Microcontamination Control, Clint Haris. "Expanding the KTC liquid filter lab allows us to increase collaboration with Korean customers and to integrate new developments into new process solutions faster."

The expansion represents Entegris' ongoing commitment to serving the Korean semiconductor manufacturing market and its continued effort to work directly with customers on a local level to solve critical issues for advanced technology processes. Entegris is the leading provider of liquid filtration and purification technologies for the most advanced semiconductor applications.

In addition to the expanded analytical and R&D liquid filtration services, Entegris' KTC also provides wet and dry chemistry development, chemistry formulation and pilot scale-up, on-site metrology with real-time reporting and microcontamination and liquid filter characterization.

SPIE Advanced Lithography

Over 20 targeted customers attended Entegris' luncheon during the SPIE Advanced Lithography conference this February. Presented by Rick Wilson and Yoshiaki Yamada, the discussion focused

Ente

Huaping Wang, Senior Engineering Manager; Russ Raschke, Senior Engineer, Entegris, Inc.

on technology challenges with the latest developments in fluid handling and filtration fields of the SEMI® industry. During the technical conference, Huaping Wang and Russ Raschke presented their paper titled: *An update on Entegris' EUV pellicle compatible EUV inner pod development.* Click here for the full abstract.



Publisher: Entegris North America
Editor: Françoise Moign
Please contact francoise.moign@entegris.com for
permission to reproduce Zero Defects articles

ENTEGRIS NORTH AMERICA

A question about Entegris products?

Call your customer service center

Tel. 800 394 4083 (toll free)

Tel. +1 952 556 4181



Cost Reduction

Improved Ion Implant Exhaust Management Reduces Energy, Capital Costs

By Steven Ballance, P.E., Facilities Engineer — Texas Instruments; Karl Olander and Joe Sweeney, Electronic Materials — Entegris, Inc.

Over the last decade, considerable efforts have been put forth by manufacturers and suppliers to help reduce costs, consumption of natural resources and, where economically viable or by mandate, to become more green in fab operations. In the early 2000s, Texas Instruments (TI) outlined an opportunity to re-think its approach around one of the largest energy and cleanroom air consumption areas in the fab — ion implant operations. Ion implanters require the largest exhaust volume of any tools used in semiconductor fabs, typically using 2500 CFM split between the gas box (400+ CFM) and the containment shell (2000+ CFM). The energy cost to replace this volume of air is ~\$8,000 per tool per year, or ~\$240K for the 30 implanters in a typical fab. In addition, the investment needed to replace this volume of clean, highly conditioned air is substantial and requires large infrastructure expenditures (Fig. 1).

Typical Ion Implanter Exhaust Flows (CFM) and Energy Costs

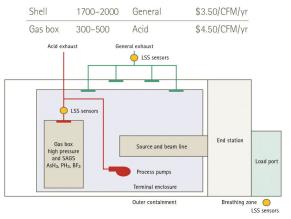


Fig. 1. Typical ion implanter exhaust flows and energy costs.

By redesigning the exhaust system based on the use of only the safest gas packaging technology — subatmospheric gas sources (SAGS), TI was able to redirect shell exhaust back into the fab and greatly reduce CO₂ emissions. Recycling the shell exhaust saved \$1.7 million in facilities capital annually, and reduced energy cost by \$470,000. Over the years, TI has replicated this design in other fabs. Figure 2 illustrates these cost savings projections.

Exhaust and Make-up Air Capital Cost Comparison for a Ten-Implanter Expansion Project	Traditional Exhaust Configuration	Reduced Exhaust Configuration	
Terminal enclosure exhaust (SCFM)	17000	Recirculated	
Gas box exhaust (SCFM)	4500	1700	
Total (SCFM)	21500	1700	
	Installation	Installation Costs (US\$)	
Galvanized steel duct	\$13,000	\$5,000	
Coated stainless steel duct*	\$100,000	\$37,000	
Exhaust fans	\$100,000	\$23,000	
Fume scrubbers	\$300,000	\$60,000	
Make-up air handlers	\$220,000	\$40,000	
Total	\$733,000	\$165,000	
Total Cost Avoidance	\$570	\$570,000	
Net Cost Avoidance Per Implanter	\$57	\$57,000	

Fig. 2. Reconfigured exhaust system amounted to \$57,000 cost avoidance per process tool.

The initial planning for reconfiguring the shell exhaust system in the new design (Fig. 3) was done to take full advantage of the safety profile of the SAGS packages. Using traditional high-pressure delivery systems in the new design wouldn't have been prudent because of the higher gas leak potential and lower safety profile. Exclusively using SAGS technologies (Fig. 4) enabled the exhaust reduction program approach.

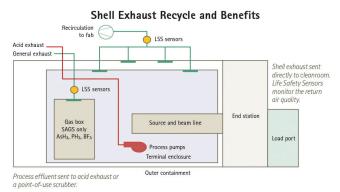


Fig. 3. New design configuration for shell exhaust recycle.

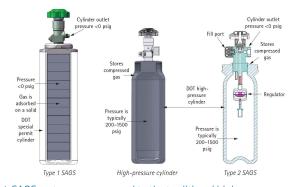


Fig. 4. SAGS systems as compared to the traditional high-pressure cylinder.

Developing an integrated exhaust system can ultimately reduce implant makeup air requirements by 98% without compromising safety. The lower exhaust requirements reduce fab operating costs, along with $\rm CO_2$ emissions. SAGS technology can also provide for gas box exhaust reductions, saving on the volumes of potentially hazardous materials that must be sent through a scrubber before being released. Further advances in exhaust/energy reduction are possible via a partnership between toolmakers, dopant suppliers and fab designers to incorporate an integrated exhaust system for ion implanters and possibly other tools. Outstanding economic and environmental gains can continue to be made — and new standards created — if manufacturers, equipment makers and suppliers work together to envision the possibilities.

This is a summary of an article that appeared in the January/February issue of Solid State Technology magazine, and is based on text, graphics, and data originally presented at the 26th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC 2015), May 3–6, 2015, Saratoga Springs, New York.

Read the full article: Link

CVD Cobalt Selective Deposition for Bottom-up, Void-free Via Fill

By Jun-Fei Zheng, Phil Chen, Ruben R. Lieten, Steve Lippy, Asa Frye, Tom Baum, and Jim O'Neill — Entegris, Inc.

In IC technology, at 10 nm node and beyond, traditional Cu dual damascene metallization faces increasing challenges for producing low-resistance and void-free Cu via fill. Copper interconnect performance degrades due to rapid increase in via resistance with reducing dimensions. Starting at about 15 nm dimensions, Cu-filled via resistance increases because of increased electron scattering at Cu grain boundaries. Furthermore, the diffusion barrier and adhesion layers (TaN and Ta, respectively) in the traditional Cu interconnect structure reduce the volume for Cu fill and thereby contribute to the increased resistivity because these materials have higher resistivity than Cu. At a given TaN/Ta thickness, the impact of these layers increases when the via dimension decreases, because they account for a greater cross-sectional area of the conductive path.

Cobalt (Co) metal, which has been used in Si technology extensively in the past for Co silicide and presently as Co liner, replacing Ta, has recently been proposed to be used as a barrier-less and liner-free metallization to replace Cu in both logic and memory applications at 10 nm node and beyond. Bottom-up selective CVD Co deposition and electroless Co plating has been attempted to achieve void-free via fill.^{1,2} This is an attractive option because bottom-up growth is the best approach to eliminate void formation and thus achieve high process yields. This approach also eliminates the higher resistivity TaN and Ta layers in the via structure. Co has intrinsically less electron scattering related resistance increase in smaller vias compared to Cu. With the via diameter at 15 nm, the barrierless and liner-free Co filled via is estimated to reduce the via resistance by 30% when compared to conventional Cu via integration. These benefits will greatly boost interconnect performance and enable aggressive technology scaling.

In this application note, we report a CVD based selective Co deposition process that achieves bottom-up via fill. A novel CVD precursor allows highly selective deposition on the Cu surface at the bottom of the vias to achieve bottom-up fill.

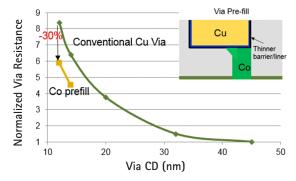


Fig. 1. Scaling of via resistance showing 30% via resistance reduction at 7 nm BEOL.

Experiments and Results

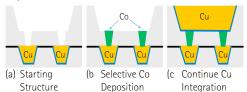
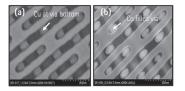


Fig. 2. Barrier/liner less Co selective deposition to fill small via.

Figure 2 illustrates the integration flow. A 28 nm node Cu dual damascene structure that has 45 nm via size at 3:1 aspect ratio, was first used to test selective Co deposition and bottom-up fill.



- Fig. 3
- (a) Top view of test structure before Co selective deposition.
- (b) After Co selective deposition.
- (c) Cross sectional view of structure with Co filled via.
- (d) 10–20 nm structure with Co pre-filled via.

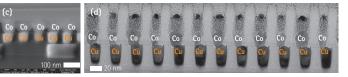


Figure 3(a) shows the SEM top view of the test structure before Co selective deposition. The test structure went through a wet surface preparation clean first, then Co selective deposition was carried out at 250°C. Figure 3(b) is the SEM top view of the structure after Co deposition. There was no Co growth observed on the ULK surface. Figure 3(c) is the cross-sectional view of the via structure filled with Co. No voids were observed because the Co growth is selective and bottom-up.

After demonstrating successful bottom-up via fill for 28 nm node structures, the scalability of this technology to 10 nm node and beyond was investigated. Fig. 3(d) shows results of Co via pre-fill in test structures of 10 to 20 nm size, which is equivalent to 5 nm and 7 nm node technology, respectively. Not only is the pre-fill void-free, but it is also self-aligned: Co pre-fill has high tolerance to via to Cu line misalignment. This robustness process is advantageous towards achieving a high-yield via fill process.

Conclusion

We have demonstrated selective Co CVD deposition on Cu surfaces to achieve bottom-up, void-free via fill scalable to 10 nm and beyond. Barrier-less and liner-free Co filled vias are expected to have 30% reduction in via resistance compared with conventional Cu filled vias with TaN/Ta layers. The Co pre-fill process has high tolerance to via misalignment. This innovative process is expected to enable high yield and high performance for advanced node BEOL interconnects.

References

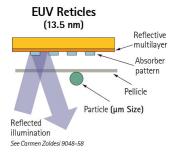
- 1. Jun-Fei Zheng, et al, Proc. of the IITC 2015. P. 265-267.
- 2. Marleen H. Van der Veen, et al, et, Proc. of the IITC 2015, p25.–27.
- P. Chen, et al, Submitted to Materials and Advanced Metallization, Brussels, Belgium, March 20th 23, 2016.

An Update on Pellicle-compatible **EUV Inner Pod Development**

By Huaping Wang, Russ Rashke, Chris Newman, Andrew Harris — Entegris, Inc.

The current EUV (Extreme Ultraviolet) reticle storage and transport solutions rely only on the EUV pod, which has an all-metal EUV inner pod (EIP) composed of a cover and a baseplate, and an outer pod to protect the EUV reticles from particle contamination. However, once the reticle is taken out of the EIP inside the lithography chamber there is no protection, which can result in particle contamination if there are particle sources inside the chamber.

Traditional photolithography reticles have a pellicle mounted to their pattern side at a distance from the surface to act as a "dust cover" and keep the particles out of focus, so that micron- and submicron-size particles do not cause lithography defects during pattern transfer to wafers. These pellicle materials are transparent to the traditional photolithography Figure 1. Illustration of an EUV light. In EUV lithography (EUVL),



pellicle for reticles.

however, the EUV light can be absorbed by most materials. Pellicles of new materials have to be developed for EUV application. Although EUV lithography has been in development for more than a decade now, EUV pellicles are only recently becoming ready for production testing. Figure 1 illustrates how an EUV pellicle works.

By 2015, EUV pellicle development has made significant progress, such that it is mature enough for production testing. For example, ~85% EUV transmission has been achieved, good thermal resistance that can withstand ≥125 W source power has been achieved, and pellicle frame design has been optimized and finalized¹. To support the implementation of the pellicle, the current EIPs need to be modified to accommodate the pellicle and the pellicle frame to the reticle, which primarily involves adding a pellicle pocket to the baseplate of the EIP.

Working closely with an EUV lithography scanner manufacturer, Entegris has developed a pelliclecompatible EUV inner pod that has passed this customer's testing and is deemed qualified for use with pellicalized reticles in scanners for early access development work. This paper presents the key design features of the Entegris pelliclecompatible EUV pod and the testing results.



Figure 2. The pellicle frame concept established the Entegris pelliclecompatible EIP design.1

Design Features of the Entegris Pellicle-compatible EUV POD **Design Considerations**

Entegris developed the pellicle-compatible EIP by modifying the existing non-pellicle baseplate. The non-pellicle baseplate is a flat plate and is designed to maintain a very small distance from the underside (also pattern side) of the reticle. For a comparison between the two, reference Figure 5.

No change to the EIP cover is required.

The required shape of the pellicle pocket in the EIP baseplate is dictated by the shape of the pellicle frame. Figure 3 shows an overlay of the pellicle pocket requirement (maximum volume) for the pellicle frame and the existing Entegris non-pellicle baseplate. There are some conflicts with the existing gripper pockets (labeled 1 in Figure 3) and sensor windows (labeled 2 in Figure 3) in the baseplate that need to be resolved in the design of the pelliclecompatible baseplate. The existing gripper pockets are higher than the required depth of the pellicle pocket, so they will need to be lowered. The sensor windows are too wide, extending too far into the pellicle pocket and are higher than the depth of the pellicle pocket. So they will need to be reduced in width and recessed farther into the baseplate.

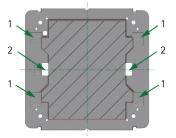


Figure 3. An overlay of the pellicle pocket requirement (shaded area) and the existing non-pellicle baseplate with conflicts highlighted.

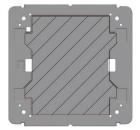


Figure 4. An overlay of the pellicle pocket requirement (shaded area) and the pellicle pocket of the Entegris pelliclecompatible EIP baseplate.

The depth of the pellicle pocket is determined by the distance of the pellicle from the reticle front surface (2.5 mm), the allowance for pellicle sag during pump down (0.5 mm or less), and a safety factor.

The weight and the center of gravity of the baseplate have to meet the SEMI and scanner manufacturer's specs.

To avoid a pellicalized reticle from being accidentally placed onto a non-pellicle EIP baseplate, a feature is needed on the EIP baseplate that can tell a sensor in a tool whether this is a pellicle-compatible EIP baseplate or not.

Design Features

The Entegris pellicle-compatible baseplate was designed by modifying the existing non-pellicle baseplate. No change to the EIP cover is required.

▶ Pellicle pocket shape and depth

The shape of the pellicle pocket is designed to both accommodate the pellicle frame and resolve conflicts with some existing features on the non-pellicle baseplate, such as the sensor windows and the gripper pockets. The sensor windows are lowered and narrowed and the gripper pockets are lowered to avoid conflict with the pellicle pocket. The final shape of the pellicle pocket is shown in Figure 4.

The pellicle pocket depth is determined such that the bottom of the pocket is at least 3.5 mm from the front side of the reticle.

Weight



Figure 5. Image comparison between Entegris pellicle-compatible EUV pod (EUV-1008P, left) and non-pellicle EUV pod (EUV-1008A, right).

For automation purposes, the weight and center of gravity of the EIP baseplates must be consistent between the non-pellicle and pellicle- compatible versions. When modifying the existing non-pellicle baseplate, material needs to be removed from the front side of the baseplate to create the pellicle pocket. This requires material to be added on the backside of the baseplate by filling some pockets (refer to Figure 6 for backside feature comparison). A comparison of the weights is provided in Table 1.

Item	1008P (Pellicle)	1008A (Non-pellicle)	SEMI E152-0214
EIP Base	0.55	0.59	0.200-0.710
EIP total	1.09	1.13	0.400-1.260
Outer Pod	2.02	2.02	1.000-2.625
Inner + Outer Pod Total	3.11	3.15	NA

Table 1. Entegris EUV pods weight comparison (kg).

▶ Pellicle-compatible baseplate sensing feature/location

As automation requires a way to differentiate pellicle vs. non-pellicle baseplates, a location on the backside of the baseplates was identified with a different depth. A distance sensor on a tool can determine what type of baseplate it is by sensing the depth at this location.

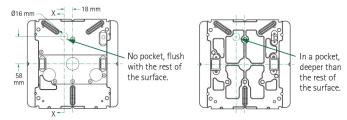


Figure 6. Baseplate sensing feature/location comparison between pelliclecompatible baseplate (left) and non-pellicle baseplate (right).

Test Results

Working closely with an EUV lithography scanner manufacturer, Entegris' pellicle-compatible EUV pod went through a full battery of tests and passed them all. The table below summarizes the results. The following paragraphs provide details about each test.

	Test	Test Result
Inspection	Mechanical measurement	Pass
	Visual inspection	Pass
Functional	Sensor target reflectivity	Pass
	Full system cycle test	Pass
Particle Adder Measurements	RH transfer path test	Pass
	In-system habitat test (venting)	Pass
Outgassing	EIP outgas test	Pass
Shipping	8-leg shipping test	Pass

Note: All tests passed the customer's specifications for pellicle-compatible pods.

Table 2. Summary of Entegris pellicle-compatible EUV pod (EUV-1008P) test results.

Inspection

The EIP baseplates are held to stringent dimensional and visual criteria. The EIP components are measured by precision measurement equipment, such as a coordinate measurement machine (CMM). Several critical dimensions are required to validate and certify a pellicle-compatible EIP, including:

- Pocket depth
- Pellicle pocket length and width
- Lateral containment feature position

Visual inspection is a critical step to validate that the EIP contains minimal defects which could potentially impact the cleanliness or environment of the reticle during transport and handling. The Entegris visual inspection specification characterizes defects including:

- Pittina
- Scratches
- Machine lines
- Stains

Functional

Reflective sensors are used in the scanners as distance sensors to tell if an EIP is properly located when it is being placed or picked up to avoid an accidental crash with end effectors. The sensor has a known linear correlation between the voltage and the distance, given a constant reflectivity of the sensor target surface. It is the EIP manufacturer's responsibility to ensure that the sensor target surface has a constant reflectivity and can produce a voltage within the scanner manufacturer's spec when measured at a nominal distance.

The sensor target reflectivity test involved measuring the voltage of a sensor that detects the reflected IR light from the target surface at a distance the same as that in the EUVL scanner. The sensor used in this test was the same as those used in this scanner manufacturer's tools.

EUV scanner system cycle tests were also completed to ensure proper handling of the EIP baseplate and covers. The EIP components were transferred from the load port through several chambers, including operations that remove the EIP cover to expose the reticle to the system.

Particle Adder Measurements

The Reticle Handler (RH) transfer path test involved many transfer steps from outside the chamber in atmospheric condition to inside the chamber under high vacuum condition, as illustrated in Figure 7. Mask blanks inside the EIPs were scanned for particle adders before and after the test cycles.

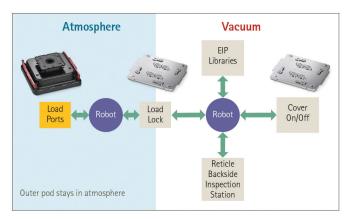


Figure 7. RH transfer path test.

The In-system habitat test (venting) involved exposing the test samples to vacuum and vent cycles inside the chamber EIP library to ensure that the EIP can protect the reticle during environmental changes in the vacuum chamber, including venting. Mask blanks inside the EIPs were scanned for particle adders before and after the test cycles.

Outgassing

The EIPs transport and store the reticles and enter the vacuum system of EUV scanner tools. The EIP is made of primarily metal components, which minimize outgassing that could compromise the reticle or EUV scanner tool environments. The EIPs were tested at a pressure of 10^{-5} mbar and the outgassing rate of H_2O , C_2H_2 of 45 to 200AMU (Atomic Mass Unit) were measured.

Shipping

The pellicle-compatible pods underwent an eight-leg shipping test including a mask blank (without a pellicle) that subjected the pods to aggressive handling conditions and, at times, excessive shock events. Each leg was nearly 1000 miles, including air and ground transportation. Mask blanks were scanned before and after the shipping test to calculate particle adders. Nearly all of the shipments experienced 50G or higher shock events as indicated by the shock watches attached to the outside of the shipping boxes.

Conclusions

Entegris has developed a pellicle-compatible EUV inner pod (EUV-1008P) that has passed an EUV lithography scanner manufacturer's tests for pellicle-compatible pods. It is approved for use with pellicalized reticles.

References

1. Zoldesi, C.; Brouns, D.; Casimiri, E.; Jansen, M.; Janssen, P.; Kramer, R.; Kruizinga, M.; Leenders, M.; Smeets, M.; Smith, D.; Wiley, J.; "A pellicle solution for EUV," SPIE Mask Lithography 2015, #9635-80.

Product Highlight

FlowPlane™ Linear Filtration Technology: Enabling Next-generation Cleanliness and Contamination Control Performance in Advanced Technology Node Applications

To meet industry demands to reduce defects, semiconductor fabs have historically had to trade off between small particle removal efficiency and high flow rate performance. This is no longer a problem with the introduction of Entegris' FlowPlane™ linear filtration technology. The ultra clean linear filter design enables faster startup times and reduced tool downtime.



The unique rectangular form factor improves flow path, and the enhanced membrane ensures low on-wafer defect levels in critical cleaning processes.

Many advanced applications require a minimum flow rate to maintain maximum cleaning process performance. Traditional radial (round) filters with next-generation membranes inevitably can no longer meet those strict performance requirements. However, FlowPlane's design delivers up to 2X the flow rate performance of a similarly sized radial filter coupled with the best particle retention available.

FlowPlane is well suited for point-of-dispense (POD) applications (installed just before the nozzle) as well as outgassing applications

that require space-constrained installation points. Moreover, the linear construction provides greater location flexibility within the tool. FlowPlane delivers the ultimate protection against particles and other defect-causing contaminants and an unparalleled level of contamination control performance.

>> Watch the FlowPlane video: link

Features	Benefits	
Optimized linear filter design	Up to 2X increase in flow rate compared to similar-size devices	
	Lowest hold up volume	
	40% space savings compared to existing designs	
Standard size and port configuration	Easy retrofit with existing device footprints	
Enhanced filter cleanliness	Faster flush-up reduces tool downtime	
	Reduced particle counts with UCM-10 cleaning technology	
Flexible installation orientation	U-line and in-line filter configurations	
	Mount at any angle without compromising venting capability in outgassing applications	
Compact device size for POD filtration	POD filtration reduces defects and improves yield	



Feedback

We value your feedback and suggestions to help us improve Zero Defects. Please send your questions, suggestions and comments to North_America_News@entegris.com

If you would like more information regarding Entegris products and services, please contact your customer service centers (page 1) or refer to Entegris on-line at www.entegris.com

Zero Defects Entegris Newsle	tter		Free Subscription Form email to North_America_News@entegris.com fax to 1 800 763 5820
Name*:		Job title*:	
Company name*:			Dept:
Address:			
Postal code:	City:		Country:
Tel. :			Send me the Zero Defects pdf file \Box
E-mail*: * required to complete			Send me the direct link of Zero Defects \Box

Entegris®, the Entegris Rings Design®, Creating a Material Advantage® and FlowPlane™ are trademarks of Entegris, Inc.

SEMI® is a trademark of Semiconductor Equipment and Materials International Corporation.

Lit. #: 9000-8084ENT-0316ZDNA ©2016 Entegris, Inc. All rights reserved.