Zero Defects

Entegris Newsletter

November 2016

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Entegris Celebrates 50 Years in Business

Entegris has struck gold. The company just turned 50 years old and achieved what is known as the "golden anniversary." The milestone was announced at one of the largest events in the semiconductor industry, the SEMICON® West trade show in San Francisco in July.

"It has been an exciting journey for us that began with the emergence of Moore's law and that has tracked the growth of the semiconductor industry into a $330 billion market," noted Bertrand Loy, president and chief executive officer of Entegris, at the semiconductor industry's annual SEMICON® West trade show in San Francisco. Mr. Loy continued: "Today, we are thrilled to be in a position to help enable the many innovations our customers continue to develop, not only in the microelectronics market but in an increasing array of industries."

Entegris was formed in 1966 as Fluoroware®, a startup company serving early microelectronics manufacturers. After merging with EMPAK in 1999 and re-branding itself Entegris, the company went public in 2000. The company expanded in 2005 with the merger with Mykrolis, a spinoff from Millipore®, and again in 2014 with the successful acquisition of ATMI®, a publicly held supplier of high-performance electronic chemicals. Today, with approximately 3,500 employees worldwide and more than $1 billion in annual revenue, Entegris stands as one of the largest global, high-performance, specialty chemical companies serving the microelectronics industry.

"Our success has been built on strong corporate values and has centered around teamwork, innovation and dedication to excellence, which have allowed us to introduce a number of market-leading product platforms throughout the years. We could not have achieved this milestone without the support of our customers and suppliers, and the dedication of our employees. I am grateful to all and I invite everyone to celebrate this milestone with us," Mr. Loy added.

Over its 50-year history, Entegris has brought hundreds of innovations to its markets, including many technology "firsts." Among its notable products are Integra® valves, Spectra™ FOUPs, PrimeLock® fittings, Torrento® liquid filters, SDS® safe gas delivery systems and NOWPak® liquid dispense systems. Industry "firsts" include the first linear wafer carrier, first wafer shipper, first wafer suspension system and the first 300 mm FOUP (wafer carrier).

"I am truly excited about what lies ahead for Entegris. We are addressing dynamic markets that increasingly rely on the kind of high-performance purity solutions we are known for. With our strong technology platform and our relentless focus on operational excellence and innovation, we look forward to continuing to deliver for our customers and our strategic partners," Mr. Loy concluded.

Yield Breakfast Forum Looks at Growth Opportunities and Calls for Increased Collaboration to Solve Advanced Memory Manufacturing Challenges

By Andrew Depoy – Brand and Marketing Communications Manager - Entegris, Inc.

While yield enhancement has always been the key to success in memory IC manufacturing, today's shrinking geometries for DRAM and NAND, as well as the emergence of 3D NAND, are making it more essential to cost effectively achieve high yields. The combination of new fabrication processes and novel materials is increasing the pressure and presenting challenges for memory makers, equipment makers and chemical/materials suppliers, collectively. These companies may need to increase their collaborative efforts across the supply chain to better solve memory yield challenges.

Industry experts from around the globe gathered to share their insights and discuss solutions at the 4th Annual Entegris Yield Breakfast Forum, held in conjunction with SEMICON West 2016 in San Francisco this past July.

"Memory is the bright spot in the whole industry," noted Wenge Yang, vice president of global marketing for Entegris and the forum host and panel discussion moderator. "It is driving rapid growth in new technologies such as 3D-NAND, X-point memory, DDR4 DRAM, etc. That's why this year's forum reflected a shift in focus to solving the challenges of new memory technologies."

Executives from the world's leading memory fabs and equipment suppliers, including Wuhan Xinxin Semiconductor Manufacturing Corp., Micron™ and Applied Materials®, along with Entegris, presented to a large audience that witnessed presentations that were followed by a lively panel discussion. Below is a brief summary of key messages from each speaker.

SPOTTING MEMORY OPPORTUNITY IN CHINA

Michael Chen, EVP and Chief Business Officer for Wuhan Xinxin Semiconductor Manufacturing Corporation (XMC), launched the first of two keynote speeches entitled, "Challenges and Opportunities of the Memory Industry in China." Chen highlighted some key indicators for growing momentum in the region as China sets out to become a tier-one semiconductor country through the creation of an entire semiconductor ecosystem. Chen noted that IC sales volume is large and growing - 18% since 2005 - and the fabless sector has experienced 34% growth, with nine fabless companies today versus one in 2009. Part of this is due to the Chinese government's massive investments.

Chen has seen evidence of this momentum surge at XMC. "We began work on 3D NAND in 2014 and we will have our first product in 2018. At the same time, we're going to do DRAM, and also some new technology like PRAM," he noted. "We can provide 3D IC stacking with logic, NAND, NOR flash, Wi-Fi and Bluetooth to serve the IoT. This is one of the capabilities we're working to complete in the next 12 months, and we're looking for partners to build up the whole ecosystem."

Speedy accomplishments such as these are what gained XMC the attention of the Chinese government and private investors, which has resulted in USD $24B of investment in the 10-year-old company.

Overall, Chen sees amazing growth opportunities in China for both fabless and integrated device manufacturers.

MINIMIZING FACILITIES IMPACTS ON FAB YIELD

"Facilities' variability has a first-order impact on yields, which will only increase in sensitivity as nodes advance below 20 nm," noted Norm Armour, Managing Director, Worldwide Facilities & Corporate EHSS at Micron, during his keynote titled, "Minimization of Facilities Impacts to Fab Yield."

Expanding on this, Armour pointed out how factors such as equipment components, operating parameters, etc., can affect fab yield and said it is critical to identify a strategy to mitigate the risk to facilities that includes monitoring the environment, equipment and processes. Modern wafer fab process tool-control methods can also be applied to facilities systems that provide real-time feedback on input variable signals, thus allowing interdiction before product is affected. Partnering with key suppliers like Entegris to leverage advanced contamination control technology is crucial for increasing yield, he stated.

Armour was previously responsible for running some of the world's most renowned fabs, including the Malta, New York logic fab of GlobalFoundries® and AMD's Fab 25 in Austin, Texas. Just recently, Armour's organization within Micron broke records with the new flagship Fab 10X in Singapore by going from ground-breaking to first-tool-installed in less than 12 months. The fab has 330,000 square feet of cleanroom, in which over 400 tools were installed in three months. It's now running 3D-NAND production.

This experience has given him some interesting experiences to draw from when understanding environmental impacts on facilities and yield. Armour noted that **airborne molecular contamination (AMC) is "public enemy No. 1" in 20 nm-node-and-below fabs around the world**.

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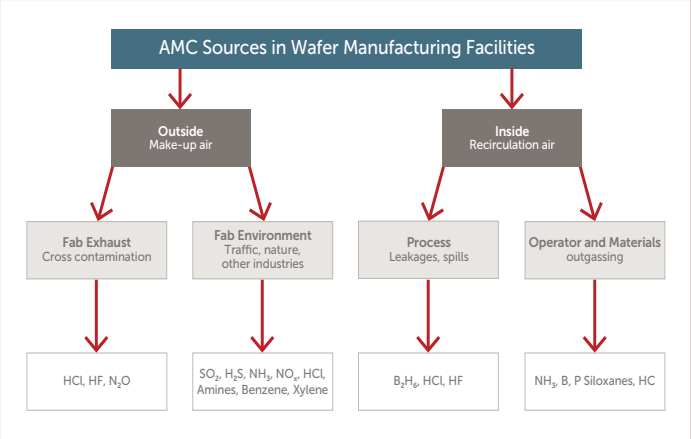


"In one case, there were forest fires in Sumatra, and the smoke was going into the atmosphere and actually went into our air intakes in a high-volume fab in Taiwan thousands of miles away. We noted a spike in hydrogen-sulfide," said Armour. "It increased our copper CMP defects, due to copper migration. After we installed higher-quality AMC filters for the make-up air units, we saw dramatic improvement in copper defects. So what is most important is that you have real-time online monitoring of AMC levels."

"Partnering with suppliers like Entegris is absolutely essential," continued Armour. "On AMCs, for example, we have had a very close partnership that developed out of a team working together at our Inotera fab in Taiwan. We used their capabilities, knowledge, and experience to help us improve the efficacy of our filtering, and they've been a great partner. There are thousands of important technologies we need to leverage now to guarantee high yields in leading-node fabs."

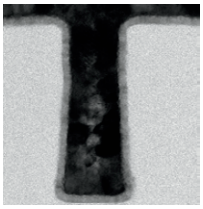
IMPACT OF STACKING ON YIELD

Er-Xuan Ping from Applied Materials has an extensive career history with memory chip manufacturing. Here, he shared the history of "cost per bit" and discussed the likely future of both 2D- and 3D-NAND high-volume manufacturing.

2D-NAND with multibit-cell technology may still have the lowest cost-per-bit today, but with improving yields, 3D-NAND is very close. With expected increases in the number of layers stacked, and with reduction in vertical gate hole pitches, each 3D-NAND fab has a roadmap to improve costs.

Ping noted that to compete with Micron in the bit density race, the primary path is increasing the density by increasing the stack. As vertical dimension scaling continues, some processes pose fundamental limitations in high aspect ratio structure, now extending to all x-y-z directions.

On the materials side, Ping said that using tungsten increases the fill qualities. However, using new or different chemistries for the fill requires a change in equipment as well; for instance, minimizing within-die variation might be impacted by loading control.



Via fill using fluorine-free tungsten

Entegris CTO, Jim O'Neill, talked about working more closely with customers to create the ideal interaction of new materials with specifically developed filtration needed to manufacture devices with sub-20 nm features. He noted, as an example, **the importance of a fluorine-free tungsten precursor for efficiency gains and the enablement of 3D NAND processes**. He mentioned the solid powder is volatile, so advanced technologies are needed for safe, stable and consistent delivery. He also spoke about the role of suppliers to use collaboration to tailor and integrate solutions, where possible, to help enable better performance.

3D NAND IS THE BIG CHALLENGE

The forum closed with a panel discussion in which panelists answered questions that ranged from specific to general.

The transition from 2D to 3D structures causes the biggest yield headache because of additional etch and CVD steps and demand for different materials. However, the panel noted it will be worth the effort, as the resulting technology is a game-changer with an upside of increasing cost-effectiveness.

Big data will have a considerable impact on managing yield. Armour noted that real-time tool data allows to adjust processes quickly to improve yield. It assists with forecasting, he claimed. In addition, vibration sensors for fault detection and wear rates could save money through immediate detection and warning, reducing downtime.

Last, there was consensus that increased, focused and detailed collaboration and joint development - worldwide and across the supply chain - is a key element to addressing advanced memory manufacturing yield challenges.

Post-CMP Cleaners for Tungsten at Advanced Nodes

By Ruben R. Lieten, Daniela White, Thomas Parson, Shining, Jeng - Entegris, Inc.

The following is a summary of a research presentation from *The 13th International Symposium on Ultra Clean Processing of Semiconductor Surfaces (UCPSS)*, held in Knokke, Belgium in September 2016. This summary is provided by one of the presentation authors, Ruben Lieten, Entegris Senior Scientist - imec Assignee.

Currently, integrated circuit manufacturers strongly depend on Chemical Mechanical Planarization (CMP) processes to planarize and remove excess dielectric layers between conducting metal layers, as well as in damascene processes involving metal interconnects (copper or tungsten) or plugs (tungsten).

Polishing slurries used in these processes are usually aqueous, low or high pH nanodispersions containing abrasive particles, oxidizers, H_2O_2 decomposition accelerators and/or tungsten corrosion protection additives. Because of this, the probability of post-CMP contaminated surfaces is very high and manufacturers usually address this issue with post-CMP cleaning formulations. With the introduction of tungsten (W) at advanced nodes, post-CMP cleaning chemistries faced their next big challenge.

WHAT ARE THE CHALLENGES FOR POST-CMP IN TUNGSTEN PROCESSES?

Particle charge in low pH tungsten CMP slurries are usually positive. The tungsten surface, however, is always negatively charged at pH >3. This leads to strong electrostatic attractions between the W surface and residual particles during post-CMP cleaning and, consequently, significant surface contamination after the CMP process, e.g., abrasive particles, organic residue, pad debris, metal cations.

THE OPTIMAL CLEANING CONCEPT

Using the Entegris PlanarClean® AG post-CMP cleaning technology, we looked at two approaches (Figure 1) to break down strong post-CMP particle electrostatic interactions on the wafer surface—as well as particle dispersion and prevention of redeposition. This included:

1. Create charge reversal at the W surface by using cleaning additives that could adsorb at the W surface and reverse the charge.
2. Create strong repulsion between a modified tungsten surface and abrasive particles while using additives that would prevent particles and organic residue from being redeposited after post-CMP cleaning.

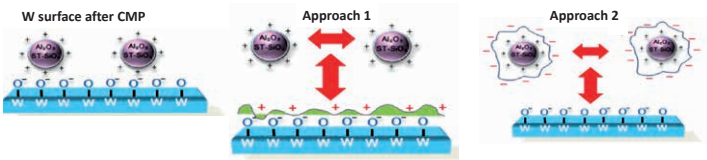


Figure 1: W Post-CMP Cleaning Formulation – Mechanistic Design Concepts

Using surface-charge reversal and electrostatic protection, Approach 1 seemed to work well. However, Approach 2 offers the best solution with two strongly-negative-charged surfaces that repulse each other and achieves the lowest adhesion.

Table 1 summarizes the main additives and their role when used in the Entegris PlanarClean AG W-100 formulation for Approach 2.

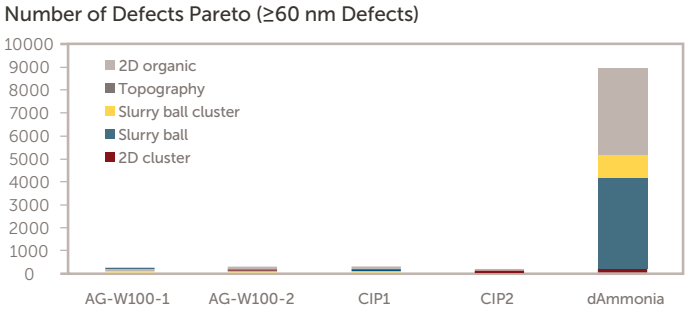
COMPONENT	FUNCTION	MECHANISM
A	Non-TMAH pH adjustor	Tungsten surface hydroxylation and good wetting. Negative surface charge surface of wafer and contamination.
B & C	Complexing agents	Surface modification of particles to prevent agglomeration and re-precipitation.
D	Dispersing agents	Prevent aggregation and control etch rate.

Table 1 - PlanarClean AG W-100 Formulation Additives List – Function and Mechanism

SUMMARY

For our experiment, we looked at several mechanistic approaches and experimental data for improving post-CMP cleaning of tungsten plugs with TiN as a "barrier/liner", and dielectric substrates SiO_2 and Si_3N_4 for use at the 10 nm technology node (metal pitch of 40 nm). Two main approaches were chosen: one using cleaning additives able to adsorb at the W surface and reverse the tungsten surface charge and one using organic additives to reverse the particle charge. The latter approach resulted in two strongly negative charged surfaces that repulsed each other and lead to the best cleaning. **PlanarClean AG W-100 (and various versions) showed excellent material compatibility and post-CMP residue removal for tungsten CMP with TiN barrier/liner.** The defect level on Si_3N_4 surfaces was significantly reduced (more than 20 times) compared to dilute ammonia cleaning (see Figure 2).

Figure 2: Defect pareto results using PlanarClean AG W-100 formulations on Si_3N_4 surfaces



For further details and study results, please see the full poster presentation here.

Presentation authors: Ruben R. Lieten, Daniela White, Thomas Parson, Shining Jenq, Don Frye, Michael White, Lieve Teugels, Herbert Struyf – "Post-CMP Cleaners for Tungsten at Advanced Nodes" – Solid State Phenomena 255, 186 (2016). Doi: 10.4028/www.scientific.net/SSP.255.186.

Study of the Impact of Thin Wafer Shipment on the Electrical Performance of Active Devices

By Anne Jourdain, Senior Integration Engineer for 3D Applications | Semiconductor Technology and Systems Department - imec

It is becoming increasingly clear that 3D integration complements semiconductor scaling in enabling higher integration density as well as heterogeneous technology integration. In addition, one can combine a wide variety of device technologies to optimize system performance. **One of the key elements within 3D technologies is the handling and processing of device wafers with sub-100 µm thicknesses.** This requires a wafer support system or carrier wafer during handling, transport and subsequent processing to allow the use of standard semiconductor equipments. But depending on the supply chain defined by the end user, it may be required that, after thin wafer processing, the expensive and fragile thin wafers have to be shipped **without carrier** to a third party (typically the OSAT) for assembly or packaging. Cracks or micro-cracks are expected to be the major failure mechanism during wafer shipping. This is even true if the wafers are thin (typically in the 50 µm range) and on film frame which is susceptible to vibrations or thermal expansion due to temperature variations during shipping.

› The problem there is how to make sure that such fragile wafers can survive the severe conditions of an external shipment and how to maintain the integrity and the electrical performance of the active devices?

We focused on testing the **Entegris E400 MFFS** package (Multi Film Frame Shipper) for this study, which is specifically adapted for handling thin wafers on film frame.

To look at the impact of shipping on the electrical performance of active wafers, several typical devices have been measured before and after thinning, and after an external shipment:

- Current of pFET transistors across 300 mm wafers
- Current of nFET transistors across 300 mm wafers
- Via resistance of daisy chains containing at least 1000 vias

The success criteria is NO difference in the above-mentioned parameters when measured before and after shipping within the accuracy of the electrical test system.

EXPERIMENTAL PLAN

The test vehicle used for this study implements a CMOS FEOL targeting the 32 nm node combined with a 65 nm two-metal-layer BEOL, and 5x50 µm via middle TSVs technology (Through Silicon Via). The presence of TSVs may increase the sensitivity of the 50 µm thin wafers to external stress.

The shipment was done between imec Belgium and Entegris Chaska (MN, US) in a E400 MFFS box, combined with a secondary package as shown in Figure 1, and wafers were returned in the same package. The wafers were fully characterized on film frame using a CM300 Probe® Station and a PDC50 Pyramid Probe Card from Cascade Microtech. This Probe Card has been specially manufactured to apply a minimum of force on the 50 µm thin wafers, and is thus perfectly adapted for extremely thin wafers testing.

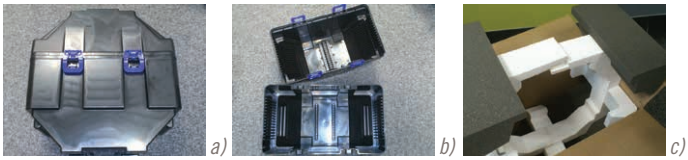


Figure 1. E400 MFFS shipping box to handle thin wafers on film frame (a) and (b). Secondary packaging to be used for E400 MFFS shipment (c).

RESULTS

Upon return in the same package, the thin wafers were visually inspected. No damage or crack could be detected. The wafers were tested again using the same test plan. To capture a maximum of micro-cracks or damage that could have been generated during the shipment, a randomly and uniform die distribution across the wafers was used in the test plan to cover about 25% of the total wafer area. Identical dies were measured before and after shipment.

The Ion current measured for the two types of transistors is consistent through the whole experiment process and does not show any variation before and after thinning, and after shipping. This clearly indicates that no damage was found on the wafers that could have impacted the electrical characteristics of the structures.

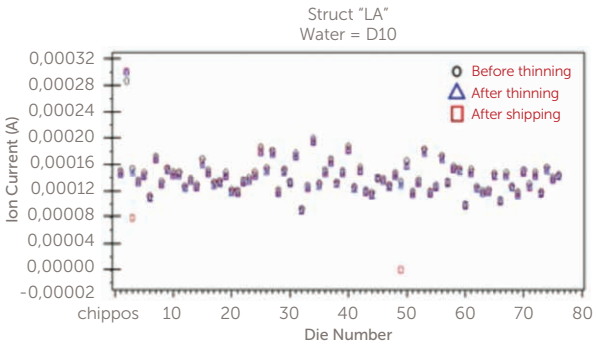


Figure 2. Ion current of nFET transistors before thinning, after thinning on film frame and after wafer shipment (Gate length: 70 nm).

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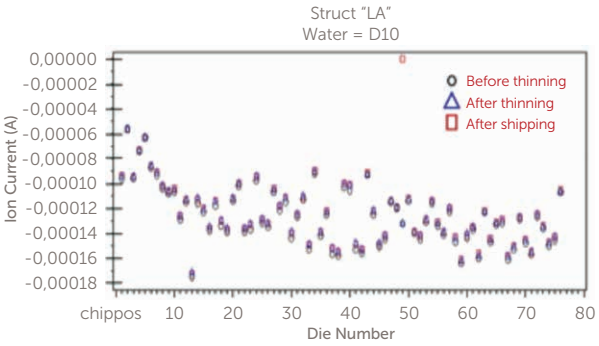

Figure 3. Ion current of pFET transistors before thinning, after thinning on film frame and after wafer shipment (Gate length: 70 nm).

This has been further confirmed by testing daisy chains structures (containing 1000 vias of 90 nm diameter). Those devices are very long structures and therefore potentially more sensitive to external stress typically caused by an external shipment (vibrations, shocks, high thermal variations). The number of surviving devices is close to 100% as shown in Figure 4.

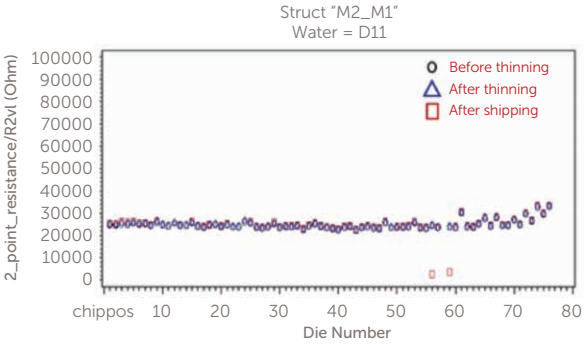

Figure 4. Daisy chain resistance measured between the two BEOL metal layers. Number of vias: 1000.

CONCLUSION

This study shows that **shipping thinned wafers on tape frame in a E400 MFFS type of box, combined with the use of a secondary package, has no measurable impact on the electrical characteristics of active devices and is a safe way to ship or transport wafers from one Fab to another**.

Reducing ESD in Semiconductor Fluoropolymer Fluid Handling Systems

By Mark Caulfield, John Leys, Jim Linder and Brett Reichow - Entegris, Inc.

The following is a summary of an article that appeared in the October issue of Solid State Technology Magazine. The full content of this piece can be seen at www.electroiq.com or this link.

Semiconductor processes, such as photolithography and wet etch and clean, have become more metal sensitive at advanced process nodes. As a result, extracted metals from chemical delivery systems can cause critical wafer defects that negatively impact process yields. To counter this negative yield impact, fabs have converted many of their stainless steel fluid handling systems that had been traditionally selected for use with flammable solvents to fluoropolymer systems. The change to fluoropolymers resulted in reduced extracted metals in the process chemicals.

However, the increased use of fluoropolymer systems creates new concerns with ESD in components such as PFA tubing. Solvents used in the semiconductor industry have low-conductivity, which enables them to generate and hold electrical charge. When these solvents are transported in fluoropolymer systems there is a significantly greater risk of static charge generation and discharge due to the nonconductive nature of the fluoropolymer materials and the low conductivity properties of the solvents. ESD events generated in fluoropolymer systems that are transferring flammable solvents can create leak paths through the tubing and possible ignition of the surrounding, potentially flammable, solvent-rich environment. An example of an ESD-created leak path through PFA tubing is shown in Figure 1.

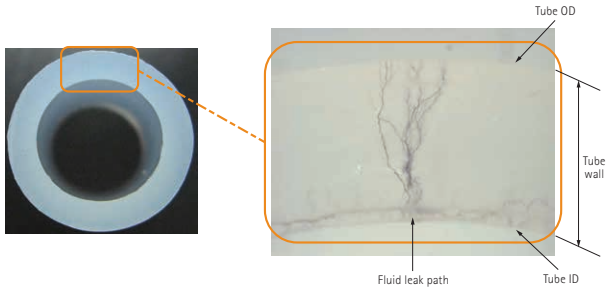

Figure 1. Example of electrical discharge through the PFA tubing wall (0.062" diameter wall thickness)

FACTORS INFLUENCING STATIC CHARGE ACCUMULATION

Low-conductivity fluid flowing in nonconductive tubing can cause charge separation at the fluid-tube wall boundary as shown in Figure 2. This separation of charge is similar to what happens when two materials move with respect to each other and transfer charge as shown in Figure 3. A charge is created as a result of the transfer of electrons and is similar to the charge that develops by walking across a carpet in dry conditions.

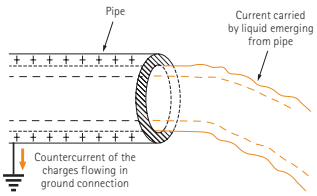

Figure 2: Charge separation at the fluid-tube wall boundary

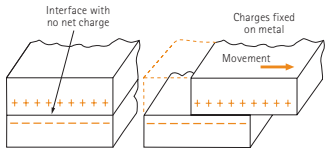

Figure 3: Charge transfer caused by movement

POTENTIAL EFFECTS OF ESD ON FLUOROPOLYMER FLUID HANDLING SYSTEMS

Dielectric strength is the measure of a material's insulating strength. NFPA 77 defines the dielectric strength as "the maximum electrical field the material can withstand without electrical breakdown." Dielectric strength is usually specified in volts/mm of thickness. As wall thickness and dielectric strength increase the tubing becomes more resistant to electrical breakdown and discharge through the tubing wall. Standard fluoropolymer tubing, such as PFA, is a very good insulator with high dielectric strength. PFA's insulating properties make it difficult to ground and also contribute to charge generation and storage in tubing systems. There have been field instances where the generated charge was able to create a discharge path through the tubing wall and cause a leak. After the electrical discharge creates the first fluid leak path, it is likely that subsequent static generation will discharge through that same leak path at lower charge levels.

ESD TUBING: PROPOSED SOLUTION FOR MITIGATING ELECTROSTATIC DISCHARGE

NFPA 77 lists several strategies for mitigating the amount of charge accumulation in electrically nonconductive pipes as a result of electrically nonconductive fluid flow. Based on one of these strategies, Entegris has developed FluoroLine® tubing with static dissipative PFA stripes on the outside of the tubing that can be connected to ground (see Figure 4). Charge accumulation that develops on the outside of the tube as a result of fluid flow is redirected to external ground paths. The purpose of having coextruded, PFA carbon stripes only on the outer diameter is to preserve the cleanliness of the tubing's pure PFA inner layer. Stripes were also used so the fluid can be seen inside the tubing.

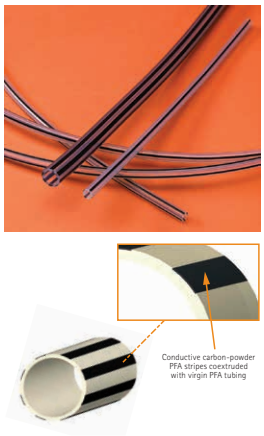

Figure 4: Entegris FluoroLine ESD tubing minimizes potential issues related to electrostatic discharge in the fab

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TESTING AND TEST PROCEDURE

Test assemblies were made to hold four-foot and 28-foot long samples of tubing that simulate how customers would use this tubing (Figure 5). The tube ends were attached to PFA fittings, the same fittings customers use, so that charge would not be discharged through the end connections. To simulate a common flow condition used by customers during the commissioning of their systems, an alternating flow of non-conducting 18 Mohm Deionized (DI) water and Extreme Clean Dry Air (XCDA® purge gas) was used. The tube was cut to length and installed in the fixtures with nonconductive PFA polymer fittings at each end. Tube samples, fittings and probe tips were wiped down with IPA after installation. DI water resistance was measured and monitored throughout the test. The electrostatic voltage field meter was placed with the probe at 1 cm distance from the tube OD.

Figure 5: Test setup of four-foot and 28-foot tube lengths

Alternating flows of DI water and XCDA were introduced to the tube and the field strength was measured at three different locations along the length of the tube. Each tube was subjected to this flow condition with and without a conductive ground strap connecting the tube to ground. In addition, the flow rate was reduced to 75%, 50% and 25% of the maximum flow rate to determine how the level of charge was affected.

TEST CONCLUSIONS

1. Grounding standard PFA tubing does not reduce the field voltage on the outside of the tube that is produced by flowing XCDA and DI water on the inside. Up to 20 KV field voltage was measured with the XCDA/DI water delivery system (Figure 6).
2. Grounding ESD PFA tubing and stainless steel does significantly reduce the field voltage on the outside of the tube that is produced by flowing XCDA and DI water flowing on the inside (Figure 6).
3. The field voltage developed along four- and 28-foot tube lengths does not vary significantly for PFA, ESD PFA and stainless steel.
4. With reduced flow rates, the maximum absolute field voltage was reduced for both grounded ESD PFA and PFA tubing.
5. No fluid leak paths were generated throughout this testing in either the PFA or ESD PFA tube.
6. The capacitance of a four-inch long PFA tube was measured to be 56 pF. Using this capacitance value and 20 KV levels of voltage measured by the field meter in this test, the energy of discharge is calculated as 11.2 mJ. This energy level exceeds the MIE of common industry fluids and would be expected to cause fumes from these fluids to ignite.

Applying this same equation to grounded ESD tubing where a maximum of 1.5 KV field was measured along with 52 pF capacitance, the discharge energy was calculated at 0.059 mJ and was below the threshold of ignition energy of the target fluids.

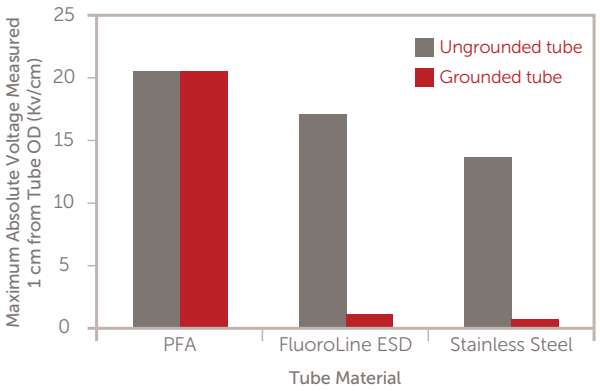

Figure 6: Field voltage on the outside of the tube

CONCLUSION

As semiconductor processes such as photolithography and wet etch and clean become more metal sensitive at advanced process nodes, fabs are converting to fluoropolymer fluid handling systems. The increased use of fluoropolymer systems creates new concerns with electrostatic discharge (ESD) in components such as PFA tubing. Electrostatic discharge increases the risks of leaks, flammability and potential explosions.

Solvents transported in fluoropolymer systems pose a significantly greater risk of static charge generation and discharge due to the nonconductive nature of the fluoropolymer materials and the frequent low-conductivity properties of the solvents. Understanding the factors that influence static charge generation and accumulation in a fluoropolymer fluid handling system, **Entegris developed an effective solution that is proven to dissipate static charge accumulation on the exterior of the tubing. Entegris' FluoroLine ESD tubing has external static dissipative PFA carbon stripes that redirect charge accumulation from the outside of the tube to external ground paths. This tubing maintains chemical purity and, when properly grounded, minimizes electrostatic discharge events, helping to increase process yields while ensuring safety.**

Fluorogard® NX Liquid Filters: Cost-effective, Hydrophobic PTFE/PFA Filters for Advanced Wet Etch and Clean Applications

Fluorogard® NX filters offer a cost-effective alternative for advanced wet etch and clean applications. Designed for aggressive aqueous chemicals and solvent applications, Fluorogard NX's hydrophobic PTFE membrane maximizes surface area to improve flow rate performance and increase device yields at elevated temperatures. Ideal for medium- to high-flow extended lifetime applications, Fluorogard NX filters remove particles from a wide range of acids, bases and other process chemicals. In addition, the PTFE/PFA fluorine resin materials and thermally bonded construction minimize chloride, metal extractables and other contaminants that can impact yield and throughput.

Fluorogard NX filters are available in various device configurations with a wide range of retention ratings to balance performance with cost of ownership. The dry configuration utilizes 15 nm and 30 nm retention ratings for solvent filtration. The optional prewet configuration ships "0.9% H_2O_2 wet", enabling rapid startup in aqueous chemicals while avoiding alcohol-chemical interactions.performance.

Features	Benefits
Retention ratings from 10 µm to 15 nm	Removes particles from a wide range of acids, bases and other process chemicals Requires minimal setup time, promoting a lower cost of ownership in advanced wet etch and clean processes Ideal for medium- to high-flow extended lifetime applications Dry configuration utilizes 15 nm and 30 nm retention ratings
Rugged materials of construction	Hydrophobic membrane's increased surface area • Improves flow rate performance with low pressure drop • Enables higher throughput and increased device yield at elevated temperatures PTFE/PFA fluorine resin materials and thermally bonded PFA construction • Ensures excellent chemical compatibility • Minimizes chloride and metals extractables that can impact process performance • Enables low particle shedding to increase yield and throughput
Cost-effective prewet cartridge filter option	Ships "0.9% H_2O_2 wet" • Allows for rapid startup in aqueous chemicals • Prevents alcohol-chemical interactions

Feedback

We value your feedback and suggestions to help us improve Zero Defects.
Please send your questions, suggestions and comments to Asia_News@entegris.com

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